

Corner-based Timing Signoff and What Is Next

Alexander Tetelbaum

Abelite Design Automation, Inc

Walnut Creek, USA

alex@abelite-da.com

ABSTRACT

The paper describes contemporary corner-based timing signoff methodology and tools and why they have problems to handle multiple global and local variations in process (transistor, wire and via parameters), voltages (including multiple V-domains that may be partially correlated), temperatures, and aging degradation during timing signoff. It discusses trends in the number of signoff corners, minimization of this number needed for signoff with avoiding a risk of silicon failure due to insufficient number of corners. The paper discusses some limitations and drawbacks of commercial STA/SSTA tools, current timing signoff methodology, optimism and pessimism of timing derating, and timing deadlock. Finally, it outlines new advanced statistical timing signoff methods that have been developed at Abelite Corporation.

Table of Contents

| | |
|---|----|
| 1. Introduction..... | 3 |
| 2. Corner-Based Timing Signoff and Corner Number..... | 4 |
| 3. Conventional Timing Signoff Methodology..... | 16 |
| 4. Advanced Timing Signoff Methods..... | 27 |
| 5. Conclusions..... | 33 |
| 6. References..... | 34 |

Table of Figures

| | | |
|-----------|--|----|
| Figure 1 | Number of timing signoff corners..... | 4 |
| Figure 2 | Illustration of delay variations in global PVT/RC space | 6 |
| Figure 3 | Process corner number evolution..... | 9 |
| Figure 4 | Illustration of delays in one cell, net, and the stage (cell & net)..... | 9 |
| Figure 5 | Illustration of delays in cells C1, C2, and sub-path $P=C1+C2$ | 10 |
| Figure 6 | Illustration of the WC-hold slack with SS and EOL model..... | 11 |
| Figure 7 | Illustration of the WC-setup slack when RC-worst model is used for wire & RC-best model is used for via..... | 12 |
| Figure 8 | Corner number after Via models are added | 12 |
| Figure 9 | Who demands multi-corner timing signoff..... | 15 |
| Figure 10 | Corner-based signoff ignores the timing yield requirement | 16 |
| Figure 11 | System performance is decreased due an excessive simplified derating..... | 17 |
| Figure 12 | Lost in SoC performance due an excessive simplified derating..... | 18 |
| Figure 13 | Illustration of possible optimism in timing..... | 20 |
| Figure 14 | Illustration of possible optimism in timing | 20 |
| Figure 15 | Illustration of hold timing yield vs. margins..... | 21 |
| Figure 16 | Illustration of possible signoff deadlock..... | 26 |
| Figure 17 | Signoff methods comparison | 32 |

1. Introduction

The corner-based timing signoff approach is a historical and traditional method that has justified a development and enhancements of conventional STA tools and signoff flows. The number of signoff corners exponentially grows along with an increase of variation sources, their magnitude, and timing margins. It becomes a bottleneck in the design flow and leads to a risk of silicon failure, an over-margining, over-design, a loss in the System-On-Chip (SoC) performance, timing yield, cost, etc. It causes a timing signoff deadlock and still does not guarantee against a silicon failure. This paper examines the situation and outlines possible solutions.

Chapter 2 discusses the corner-based timing signoff methodology and the corner number used in this methodology. It explains why the corner number grows exponentially and is becoming a challenge. It increases the duration of the timing signoff, makes timing closure difficult and worsens most of design metrics. The corner-based timing signoff is a justification for the current design flow and contemporary STA/SSTA signoff tools. It has multiple impacts on the design flow, Time-to-Market (TTM), cost, SoC performance F, timing yield Y, etc. It becomes a problem for getting the most benefits from moving to next advanced technology nodes.

Chapter 3 discusses the conventional timing signoff methodology in details. It starts with a definition of the current timing closure and the timing yield. It shows that the conventional timing signoff does not support the timing yield as a design signoff requirement and it becomes a challenge. Then, timing derating (margins) methods of contemporary STA tools, which should cover for variations, are considered. An increase of variation sources and their magnitude leads to losses in the SoC performance and diminishes other design metrics. Some limitations and drawbacks of current derating methods are considered and, then, it is shown that Statistical STA (SSTA) tools provide a partial solution but are not panacea. Later, in this chapter, we consider a signoff optimism and conservatism (pessimism), different variability sources and, finally, the timing signoff deadlock.

Chapter 4 outlines new advanced timing signoff paradigms and methods that have been mainly developed at Abelite Corp. (POCV is Synopsys' upcoming method). Namely, it discusses the following 4 options that may be adopted by the EDA industry: Option 1—Enhancing the AOCV derating method; Option 2— Switching to the Parametric OCV (POSV); Option 3— Developing pseudo-statistical tools; Option 4— Developing statistical Monte Carlo-based tools. Options (1) and (2) may be combined with minimizing the corner number and using a detailed examination of variations in found risky (timing critical) paths. Options (1), (2) and partially (3) may be considered if a company is using the corner-based signoff and this is a must-to-use method for the company no matter what it takes. Options (3) and (4) may be more beneficial as it is shown in the chapter. Finally, Options (3) and (4) are computationally expensive, especially Option 4 and there is a challenge with their validation. It is not likely they will replace the AOCV/POCV in the best-in-class PrimeTime [1] and ICC [2] tools, but they can be used on top of PrimeTime (after a PT run).

Chapter 5 has our conclusions on sharing our experience and knowledge on the status and new signoff methodologies, on an emerging advanced signoff philosophy, and, finally, it provides a summary of this paper.

2. Corner-Based Timing Signoff and Corner Number

System design companies and design houses continue to use the traditional corner-based signoff approach that has been developed more than 40+ years ago and has since remained mainly unchanged as an industry paradigm. Initially it had 2 corners, namely Worst Case (WC) and Best Case (BC) with the maximum and minimum cell delay respectively. Note that wire and via delays were negligible. Later, the number of corners increased to 4 and after that it has been growing exponentially, especially during last 10-15 years when technology moved to the deep sub-micron dimensions. Figure below illustrates the spread of timing signoff corners used in different design companies and some predictions for the future:

- Without Via RC models (the current approach)
- 2013 (Currently): From 12 to 126
- 2020 (Prediction, if no change in signoff paradigm): From 16 to 248

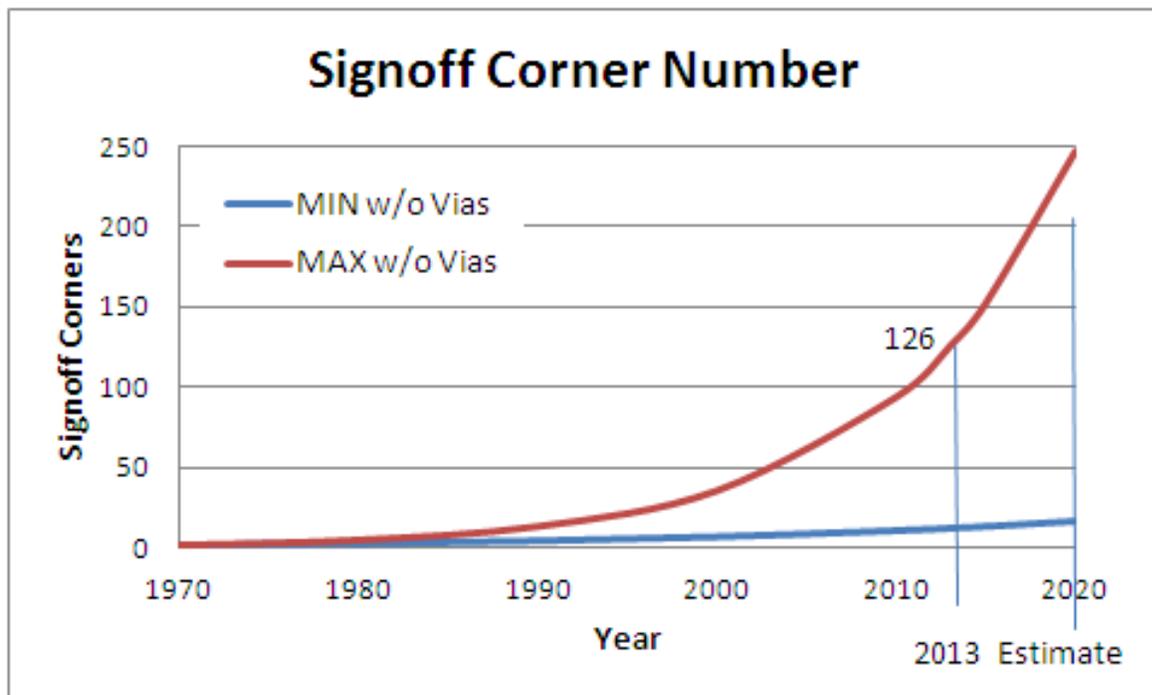


Figure 1 Number of timing signoff corners

Let's consider the number of corners needed for the signoff in more details. During last 10-15 years, when the Electronic industry and technology have moved to the deep sub-micron nodes (28nm and below), the situation with the corner number has drastically changed. On one hand, designs (SoC) have increased in size and became more complex in their structure, functionality and operational modes (functional, test, scan, sleep, wakeup, audio, video, and network), with

multi voltage domains, clock gating, etc. On the other hand, a significant increase of delays in wires and recently in vias, new physical effects in cells and metal (FinFet, Temperature inversion, DPT, Age Degradation, etc.) have led to new sources of variation and an increase in variation magnitudes (global and local). It was confirmed by many studies that smaller geometries have had a higher variability. The need for so many corners is due to a fact that it's not just enough to look at the maximum or the minimum sub-path (launch, data, and capture) delay: The worst slack may occur as a combination of maximum and minimum sub-path delays.

One can easily see (Figure above) a corner number exposure due to the current signoff paradigm: Signoff must be performed at numerous (the most important) global PVT/RC corners. Note that at each global corner, the whole die experiences the same:

- External Voltage (like Minimum, Typical, Maximum)
- Temperature (like Minimum, Typical, Maximum)
- Process shifts (independent) in:
 - Transistors: {Slow: SS, Typical: TT, Fast: FF or mixed SF & FS for (p-n) uncorrelated slow/fast combinations}
 - Interconnects {4 RC-extremes & RC-typical} & Vias {max/min/typ cap/resistance} incorporated into the interconnect model

It is important to find and use the minimum number N_{corners} of corners because:

- Runtime and Turn Around Time (TAT) are increasing with the N_{corners} growth
- Each corner may need its own OCV/AOCV timing margins and finding them is a challenging task

Note that it is not trivial to find the minimum N_{corners} and still guarantee that we cover enough points in the Global Variation Space, which is illustrated in Figure below as a 2D-space:

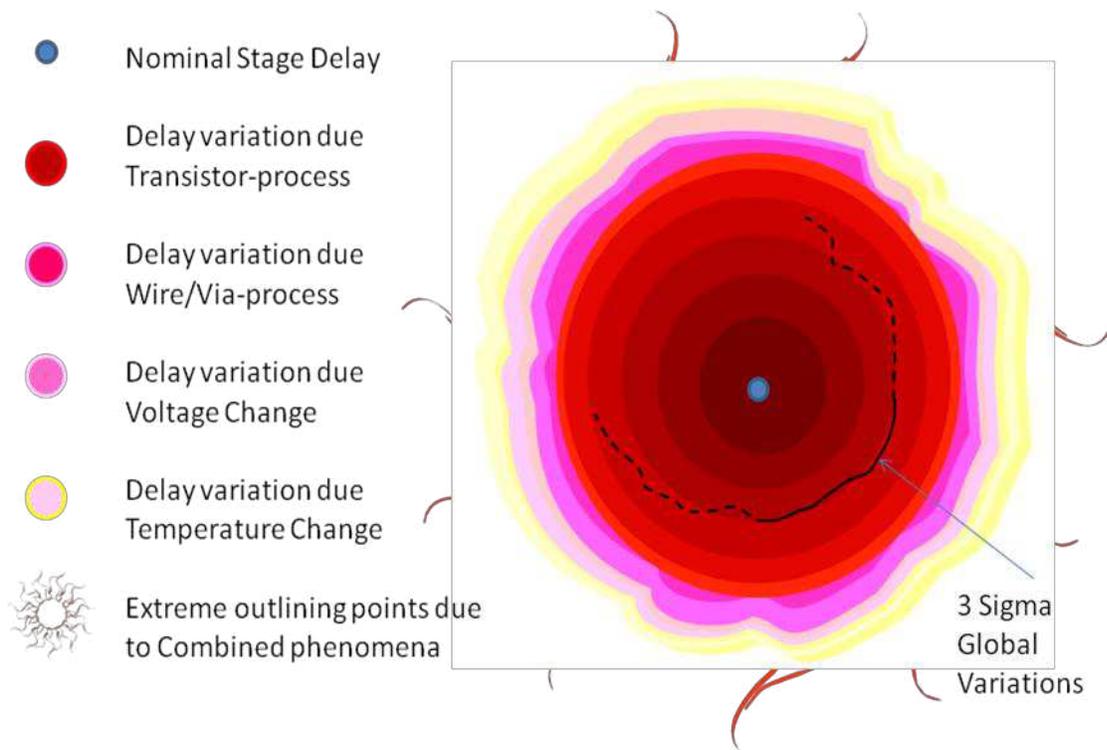


Figure 2 Illustration of delay variations in global PVT/RC space

In the above figure, axe X shows, for example, stage delay $T(V,P,T,\dots)$ as a function of a voltage variation $V-V_0$ from nominal value V_0 , axe Y shows stage delay as a function of a process variation $P-P_0$ from nominal value P_0 , and variations in other factors are impacting stage delay too.

Let's start with the following initial (and historical) **Corner Definition**: Corner is an extreme point in the PVT/RC space where cell and net delays have extreme values—all are the maximum or all are the minimum. [This definition should not be confused with the correct way contemporary STA tools work. For example, PrimeTime uses a mix of maximum and minimum delays, e.g. for setup check it uses maximum launch clock and data delay and minimum capture clock delay. The corner is a particular one cell library and RC-model specified for STA run. Thus, maximum data delay means the delay from the specified library plus some timing derate.] This Definition is not correct because all maximum or all minimum path delays may not cause all timing violations: Slack is a function of 3 sub-path delays (the clocks and the data sub-path). The only important is the Timing Slack and its minimum value that must be more than zero (to avoid a timing violation):

- The Minimum Slack is a more complex function of PVT/RC than the extreme one sub-path delay
- A mixture of the cells/nets maximum and minimum delays in the same sub-path may produce the worst slack (these are corner delays, not timing derates)

- The Nominal (Typical) cell/net delays are extremely important and must be included into corners, because most chips will have their delays around this corner. E.g. the nominal process corner is one of required corners in the GlobalFoundries reference design flow.

Thus, the current WC/BC and RC/C-best/worst terminology may be confusing and misleading. Now, let's formulate a new true **Corner Definition**: Corner is a point in the PVT/RC/+ space where cell/net delays have extreme (and optionally nominal) values—all cell delays are the maximum or minimum and all net delays are the maximum or minimum independently. It means that, for example, all cell delays may be the maximum and all net delay may be the minimum. Sign + after PVT/RC indicates that other additional factors may be present in the corner description. Also, we will discuss later that net delay is actually wire and via delays and they must be considered independent too.

Let's estimate the **total corner number**. We will start with taking into account only the extreme points (without the nominal points for now) for each X variation factor $X = (P, V, T, RC)$ assuming a linear and fully scalable cell/net delay behavior as a function of X. Then, we will need to initially include the following corners:

$$\text{CORNERS} = \{P: SS \ \& \ FF\} \times \{V: \text{Min} \ \& \ \text{Max}\} \times \{T: \text{Min} \ \& \ \text{Max}\} \\ \times \{RC: RC_{\text{best}}, C_{\text{best}}, RC_{\text{worst}}, C_{\text{worst}}\}$$

It constitutes **32** ($2 \times 2 \times 2 \times 4$) initial PVT/RC corners.

Note that nominal points are not explicitly covered by the above extreme points. If we add the nominal (typical) points, then Corners are:

$$\{P: SS \ \& \ FF \ \& \ TT\} \times \{V: \text{Min} \ \& \ \text{Max} \ \& \ \text{Nom}\} \times \{T: \text{Min} \ \& \ \text{Max} \ \& \ \text{Nom}\} \\ \times \{RC: RC_{\text{best}}, C_{\text{best}}, RC_{\text{worst}}, C_{\text{worst}}, RC_{\text{typ}}\}$$

It constitutes **135** ($3 \times 3 \times 3 \times 5$) PVT/RC corners.

Now, if we take into account that process corners $\{P: SF \ \& \ FS\}$ may produce the worst slack for some paths, then the number of basic corners is in the range from **64** ($4 \times 2 \times 2 \times 4$) to **225** ($5 \times 3 \times 3 \times 5$) for corners without nominal points and with these points respectively. There is a need to add even more corners as we will show later.

Note that I. Katz has stated [2] that “*Finding the right corners to run is a major headache: Multiply the 5 standard process corners (SS, SF, FF, FS, TT), by 2 temperature points, by 4 metal points, and by 4 voltage points. This gives $5 \times 2 \times 4 \times 4 = 160$ corners. There are ways to reduce the number of combinations (for example, only run slow metal at SS for your max frequency), so no one is running timing at all 160 corners all the time – but you're still running a much larger MCM set than in the past.*” Let's briefly comment on his estimation:

- It may be risky to remove any so-called “redundant” (or dominated, or less important, etc.) corners. For example, SS + Fast-Metal is needed for the setup check, because a violation may happen in a path where launch and data paths are cell-delay dominated and capture is metal-delay dominated. So, using only SS + Slow-Metal may lead to missing violations.

- The above corner number ignores a need for more corners to take into account the Aging Degradation (AD), multi-voltage non-correlated or partially correlated domains (supplies), the temperature inversion, other effects (like the NTBI, Hot electron injection, etc.), FinFet, DPT (Double Pattern Technology), etc., which may produce the extreme delays in some intermediate points.
- Some companies have already used 126 PVT corners
- We will need to multiple the above number by the number of modes (functional, test, etc.) too

Thus, there may be a need for all the above corners (and even more corners) [6], because different paths have different structures/properties and may show the worst slack in different corners. Note that usually each path has the worst slack only at 3-4 (less than 10) corners, but these corners are different for different paths and it's not trivial to determine them.

Advanced technologies have even more corners across the entire process window as one can see at the Global Foundries website. Next Figure illustrates an evolution in the process corner number and also shows that n- and p-transistors become less and less correlated. It means that the die can have any combinations of slow and fast transistors. Thus, if we take into account that there are 10/11 process corners (without and with the TT corner respectively), then the number of basic corners is in the range from **160** ($10 \times 2 \times 2 \times 4$) to **495** ($11 \times 3 \times 3 \times 5$) for corners without nominal points and with these points respectively. In reality, we will need to add more corners and examples and a justification will be shown below.

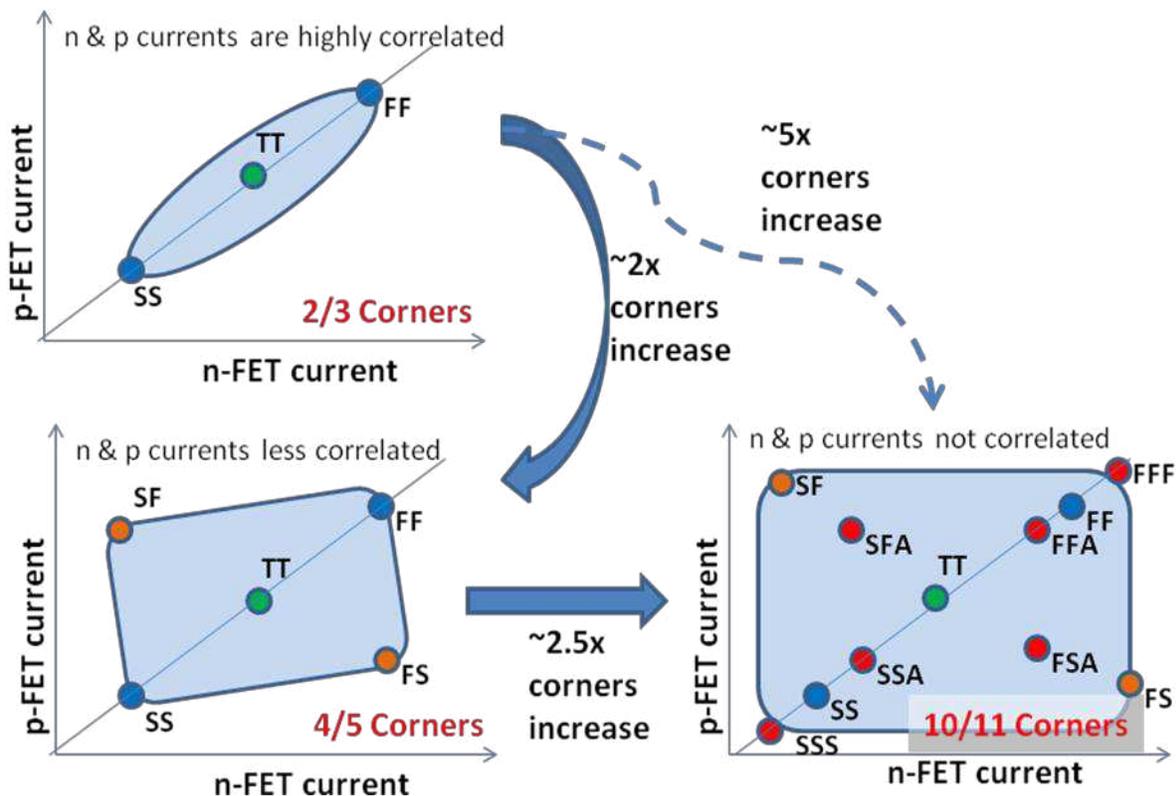


Figure 3 Process corner number evolution

Even with so many corners (160-495), there is no guarantee that we do not miss some violations due to non-linearity (like the cell delay vs. voltage) and even a non-monotonic behavior (like the temperature-inversion) for some X-factors (properties), and because of a non-perfectness of conventional tools and derating methods, and ignoring some physical phenomena like correlations. Let's illustrate it on considering the temperature inversion (T-inversion [7]):

- It is not enough to consider only two or even three temperature points T because the extreme stage/sub-path delays (see first Figure below) may occur at any temperature $T_{min} < T < T_{max}$ due to:
 - Temperature inversion effect
 - Distribution of delays between cells and nets
- The delay change is ~1-3% for each 10C temperature change and it increases for each next technology node
- Second Figure below shows an example of delays in cells C1 and C2 and the total sub-path delay, where the sub-path includes cells C1 and C2. Note that the sub-path delay is not a monotonic function of T .

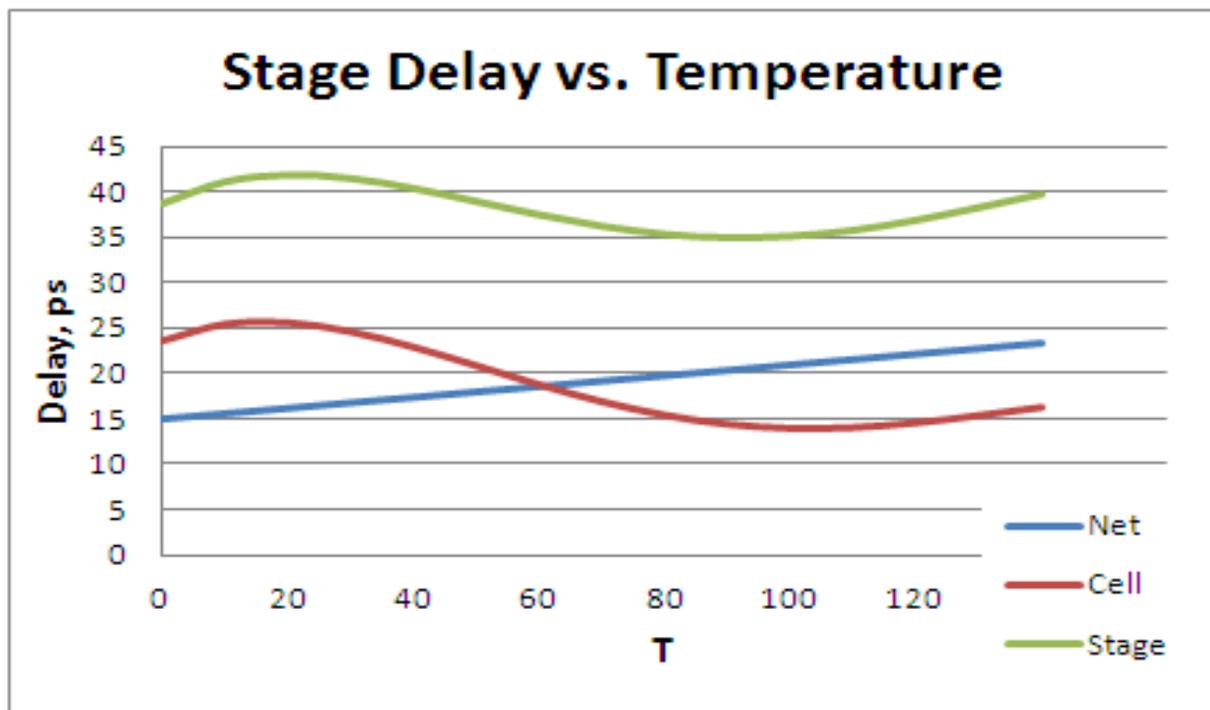


Figure 4 Illustration of delays in one cell, net, and the stage (cell & net)

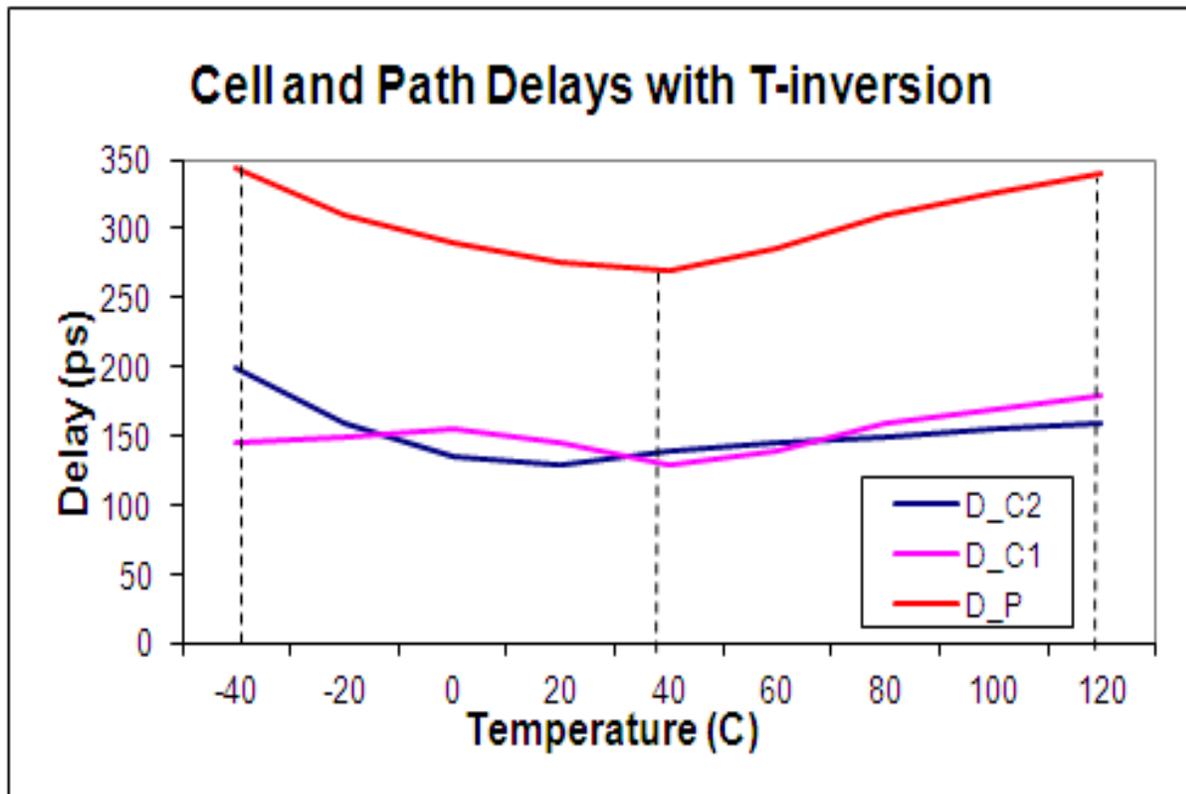


Figure 5 Illustration of delays in cells C1, C2, and sub-path P=C1+C2

Now, let's consider an Extended number of global corners. Considering only (P, V, T, RC) X-factors may be not enough. We will need to add at least two more points for Aging Degradation (AD): the BOL (Beginning-Of-Life) and the EOL (End-Of-Life). Then, Extended set of corners will include at least the following corners:

$$\{P: SS, TT, FF, SF, FS\} \times \{V: Min, Nom, Max\} \times \{T: Min, Nom, Max\} \times \{RC: RC_{best}, C_{best}, RC_{typ}, RC_{worst}, C_{worst}\} \times \{BOL, EOL\}$$

This constitutes **450** ($5 \times 3 \times 3 \times 5 \times 2$) extended corners. Note that one can doubt if we really need to run BOL and EOL at all the PVT corner points and is it fair to multiply all corners by 2 as shown here. The answer is "yes we need" and an explanation is similar to already used for some other X-factors—most corners may not need to be run for BOL and EOL for typical paths, but there may be special not typical path structures (with cell- or net-delay dominations in different sub-paths) that need not "typical" age model. Let's consider one example for hold check. A common mistake: There is no need for using SS library & EOL model, because all cell delays become slower. In reality, for some rare path structures, SS & EOL model is needed, because a violation may occur in a path where the launch and data paths are metal-delay dominated and the capture is cell-delay dominated. See this example below.

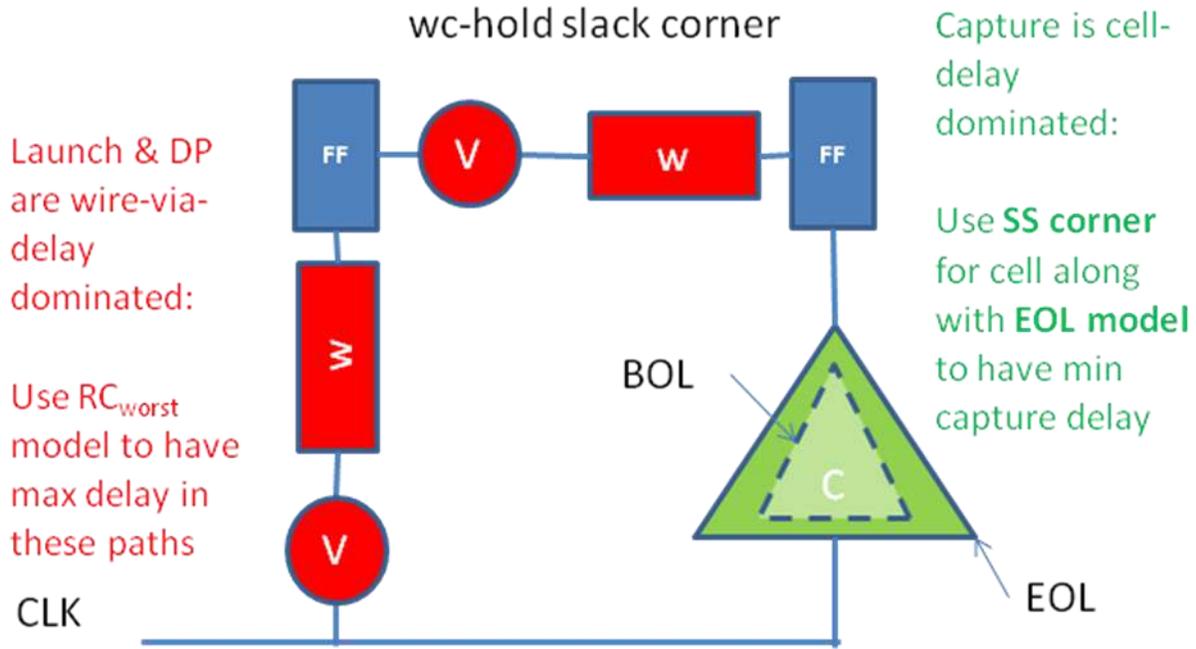


Figure 6 Illustration of the WC-hold slack with SS and EOL model

Actually, even more corners may be needed. First of all, let's start with a via corners consideration. There is a need to add Vias corners (or via RC-models) that are similar to the current wire/via RC models. Vias are independent and not practically correlated with RC-wire models. Possible Via models are:

$$\{\text{RC-via: } VRC_{\text{best}}, VC_{\text{best}}, VRC_{\text{worst}}, VC_{\text{worst}}, VRC_{\text{typ}}\}$$

Figure below illustrates the worst-case situation (corresponding to the minimum setup slack) when the RC-worst model is used for wires and the RC-best model is used for vias. In this pictogram, we use triangles to represent cell delays, rectangles for wire delays and circles for via delays. The size of each shape is proportional to the corresponding delay. Thus, if any shape is absent, it means zero delay of this type. In example under discussion, launch and data paths have big wire delays with almost no via delays; and cell delays are irrelevant here. The capture path has big via delays with almost no wire delays; and cell delays are irrelevant here. We will need to separate wire RC-models and via RC-models. We can still continue using the current notations:

$$\{\text{RC-wire: } RC_{\text{best}}, C_{\text{best}}, RC_{\text{worst}}, C_{\text{worst}}, RC_{\text{typ}}\}$$

for wire RC-models, but they will now represent only wire behavior.

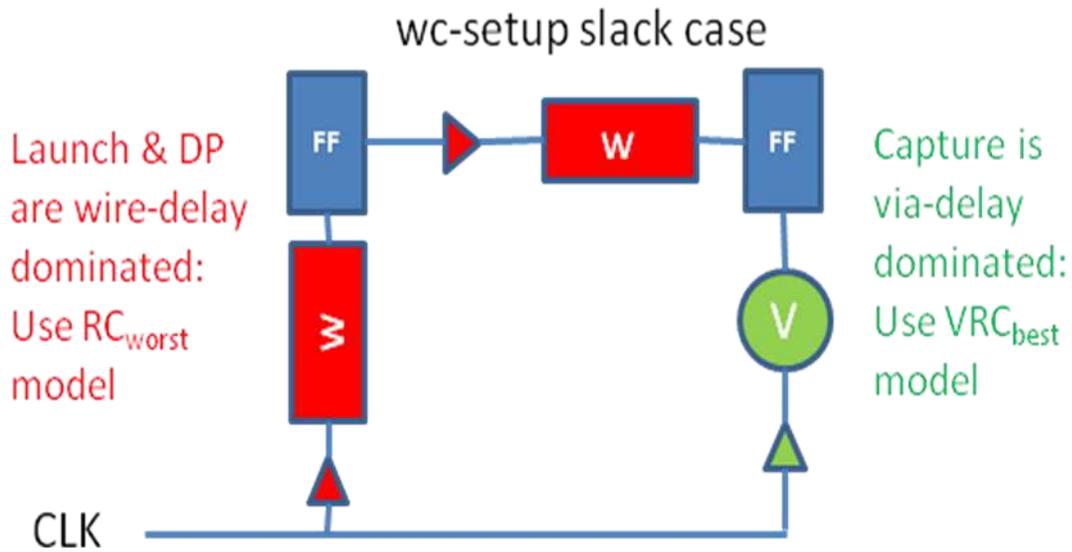


Figure 7 Illustration of the WC-setup slack when RC-worst model is used for wire & RC-best model is used for via

Adding the via models will increase the corner number by 4-5x—see Figure below.

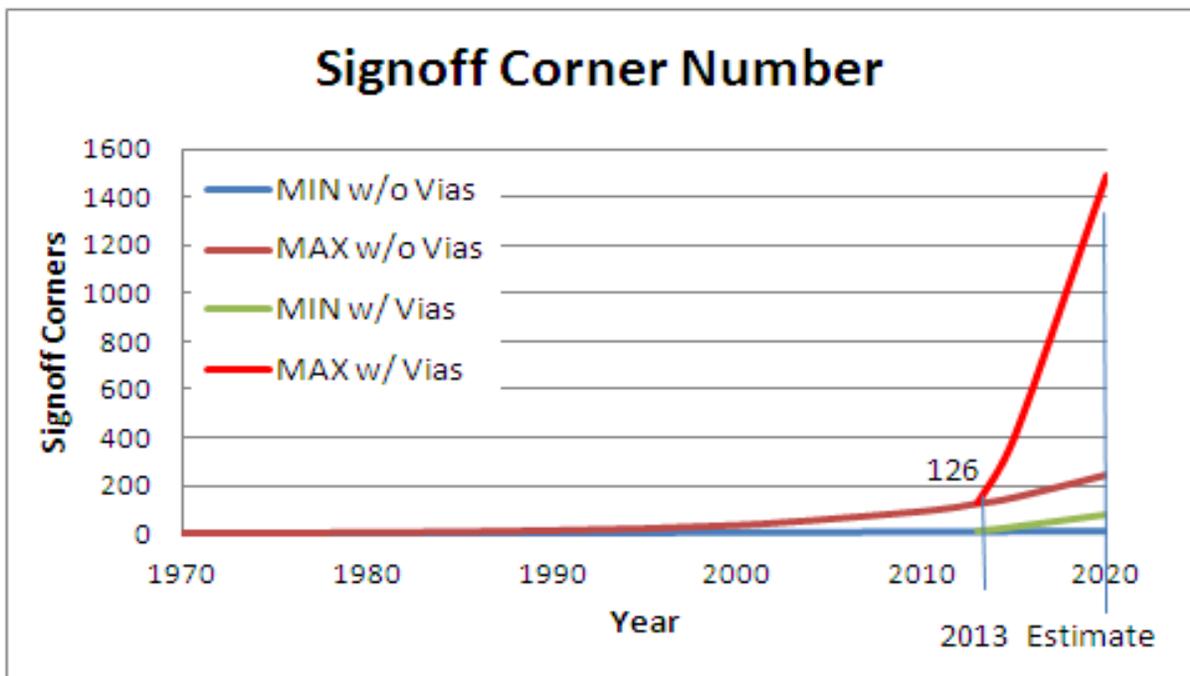


Figure 8 Corner number after Via models are added

Even more corners are needed for advanced 10-20nm technologies due to:

- Temperature inversion (may require more than 3 points)
- Non-linearity in voltage
- Designs with multi-voltage domains (in low power designs) may require considering several important combinations of voltages in the V-domains
- Additional voltages for over- and under-drive design modes
- DPT (Double Pattern Technology) may add new corners
- Via capacitance corners (additionally to resistance corners) due to using wide vias
- Using FinFET transistors with 3D structure may contribute to corner numbers and may decrease model accuracy

Using so many PVT/RC/Via corners (>1000) will be not acceptable from the design time and costs considerations. Additionally, the number of signoff scenarios is a product of corners and modes (functional, test, etc.) and becomes too big to be handled by the IC Compiler (ICC) or PrimeTime (PT). The below are 2011-release numbers, which likely were improved later:

- IC Compiler is OK up to 20 scenarios
- PrimeTime is OK up to 100 scenarios

Still, these numbers cannot catch up with the corner number growth. The runtime has become a serious issue too.

Finally, the corner number is related to the signoff level of confidence. The current signoff assumes the 3-sigma level of confidence, where all corner libraries are characterized with ± 3 sigma variations. Unfortunately, conventional STA tools and a used timing derating mechanism ignore the number N_{CR} of timing critical paths in the design. This number is critical and may actually require up to 4+ sigma level of confidence during the signoff for a specific corner, because the sigma level is a function of N_{CR} . Using a combination of the 3-sigma cell process corner and the 3-sigma metal corner may be reasonable and needed for some paths where there is a cell and/or net delay domination in clocks and data sub-paths. Still, in most typical paths, which have comparable delays in cells and nets, using multiple extreme signoff corners (PVT, metal, AD, etc.) may lead to an excessive level of confidence, much beyond 5-6 sigma.

Some companies believe that their current signoff is at the 27-sigma level. We do not know how they come up with this estimation, but can speculate that they have considered main design/technology parameters/properties like electron mobility, dopant, transistor geometry properties, etc.; plus the wire width, height, dielectric thickness, etc.; plus the via geometry properties, etc. and, then, each corner was created as a combination of 3-sigma variations for each parameter. This estimation of confidence level is not correct and is too pessimistic. E.g. traditionally all parameters that contribute to transistor variations are combined in such a way that the total process variation is at 3-sigma (and each parameter has less variation than 3 sigma).

Summarizing the above, we can say that design companies currently use 12-126 corners. For example, one leading company does signoff with 76 corners. Another, even more famous company, uses 126 corners. According to our estimates it corresponds to 6-10-sigma level of confi-

dence. Still, a violation can be missed due to drawbacks in signoff methodology/tools [5, 12]. It is still true for 100 and more corners. The questions are: How many and which corners we need? Is using the 3-sigma confidence is enough even though it is used for ages in many areas? We know that Solido Inc. recommends the 6-sigma for memory failures [11], but is it a right approach for the slack estimation and timing yield? Note that memories have millions of components and consider events (or individual failures) rather than a combined metric (like the sub-path delay or the slack). A failure in a path is a signoff event and we need to consider all paths. But is using K -sigma ≥ 3 signoff with multiple sources/factors of variations (each with 3-sigma variations) pessimistic? All these questions contributed to signoff “paranoia” and have led to even more pessimistic methods of the signoff with a numerous corner number and increased margins.

As a result, each new technology node requires more corners and increased timing derates (margins). These margins also were additionally increased to cover for libraries and EDA tools inaccuracies due to their imperfectness and approximate methods of timing derating, for example, ignoring correlations between cells and between wires and vias.

Thus, a challenge is that that number of corners grows exponentially and it makes closing timing a very difficult task:

- Time and efforts is growing almost proportionally to the corner number
- There is a risk to miss violations
- Most paths are estimated pessimistically
- Time and disk space is growing significantly for the corner libraries and characterization

Now, we conclude on the number of corners and confidence:

- Most companies are using an ever increasing number of timing signoff corners
- There is no need in most of these corners for each path
- Still, some violations may be overlooked due to ignoring some corners for a few paths
- The more corners are used, the more pessimistic is the signoff in average
- Current multi-corner signoff approach produces the timing yield confidence much higher than 3-sigma typical recommendation:
 - This confidence is in range [4-8]-sigma
 - Limitations in timing derating and unjustified two-digits derates (margins), which often are 20%+ or even more, add to a signoff pessimism
- Much more powerful and sophisticated statistical methods are needed to replace the corner-based signoff

The corner-based signoff approach has been a justification for a development and wide use of STA tools like PrimeTime, which has been a milestone in the EDA industry and the Electronic design industry. It has guided the EDA industry in timing signoff: a development and non-stop improvements of STA, SSTA, extraction, Spice-like, characterization and other tools. For example, Synopsys has developed Multi Corner Multi Mode (MCMM) analysis that is very useful and powerful, but has its limitations too because it can handle only subset of all corners/modes/ scenarios and, thus, “... *some scenarios and violations may be missed*” [3].

Note, that the corner-based signoff is the best and the only commercial approach we have in the industry for now (not counting some emerging new statistical methods and tools we will discuss later).

Thus, a challenge is that the historical signoff approach used in design companies (both SoC design and design houses) poorly “advices” the EDA industry what tools and signoff methodologies to provide and, at the same time, the existing EDA tools impose the contemporary design flow and the existing (historical) timing signoff paradigm. A similar situation exists between design companies and foundries: the design companies request die data and specs for their signoff corners and foundries request (in their white papers and specs) that Systems-on-Chip (SoC) to be functional at all those corners. Next Figure illustrates the current situation. It is no longer possible to say who now insists on using multi-corner signoff—and it has become a chicken and eggs dilemma. Finally, the EDA industry claims that design houses and foundries demand those tools to support the multi-corner signoff. So the EDA industry continues to enhance the corner-based method. This challenge has multiple impacts on a design flow, Time-to-Market (TTM), costs, SoC performance F, timing yield Y, etc., which we will consider below.

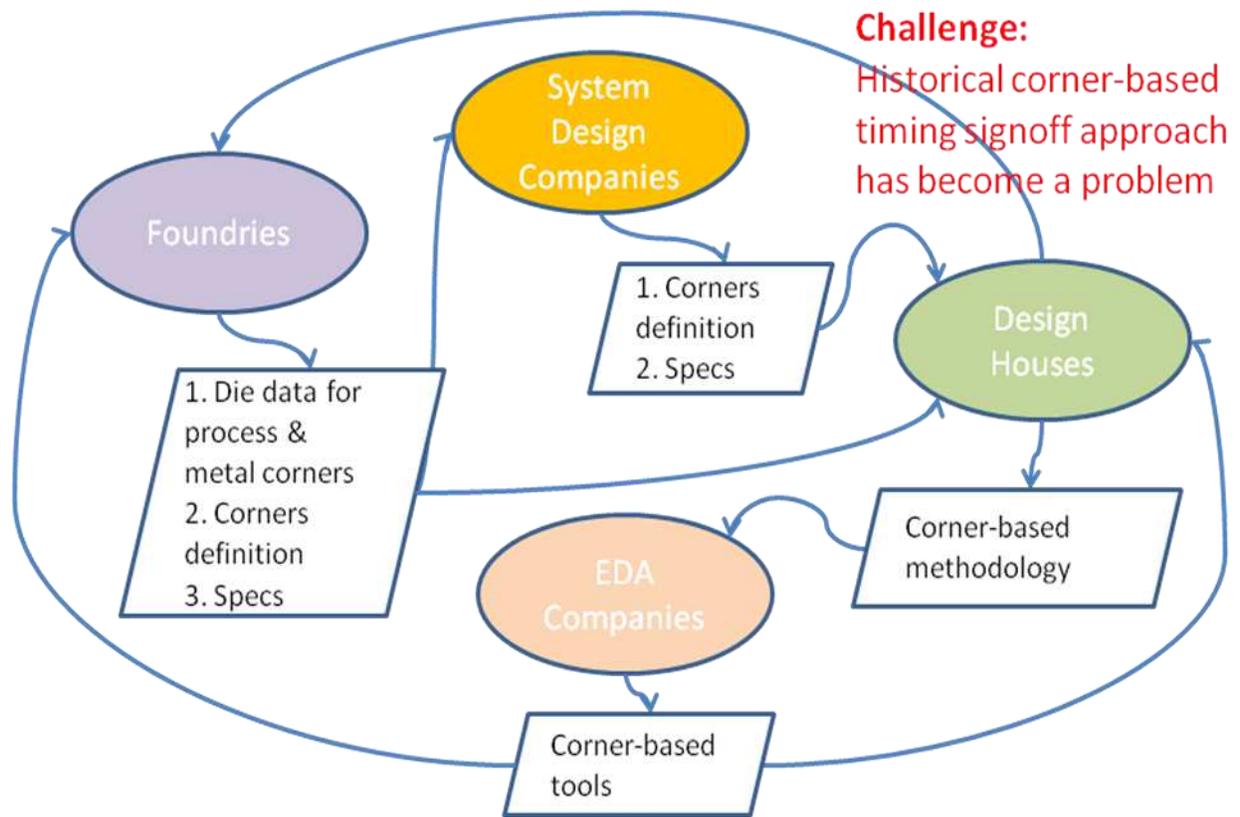


Figure 9 Who demands multi-corner timing signoff

3. Conventional Timing Signoff Methodology

Timing Closure

The conventional timing closure means that all timing violators at all corners must be fixed. Presumably, it delivers 100% timing yield or a very high yield. Note that the timing yield should not be confused with the “die yield” term, which is related to presence of manufacture defects. It is important to state that there is no such case when we can have 100% of working silicon—it means that all dies (without defects) are functional with a specified performance at all extreme corners. Moreover, not all SoC need to have a very high timing yield—it’s rather a business consideration and the yield can be traded-off for performance or a TTM reduction. Note that the defect yield is at level of 60-70% and a very high timing yield cannot improve it. It’s about time when the timing yield Y must become a part of the specification. Currently, it is a poorly formulated task to obtain a timing closure with a target performance with some excellent or good or poor, but an unknown (not specified) timing yield. Unfortunately, the conventional timing signoff does not support the timing yield as a design signoff requirement and it becomes a challenge. Also, the timing yield is not estimated during the signoff and may cause a problem later—namely, low yield and less working parts than expected. As an example, “*Apple iPhone 5S demand is currently limited to the availability of adequate silicon – their designers hit timing-closure at spec, but variability is still there.*” [2]. Figure below illustrates this challenge.

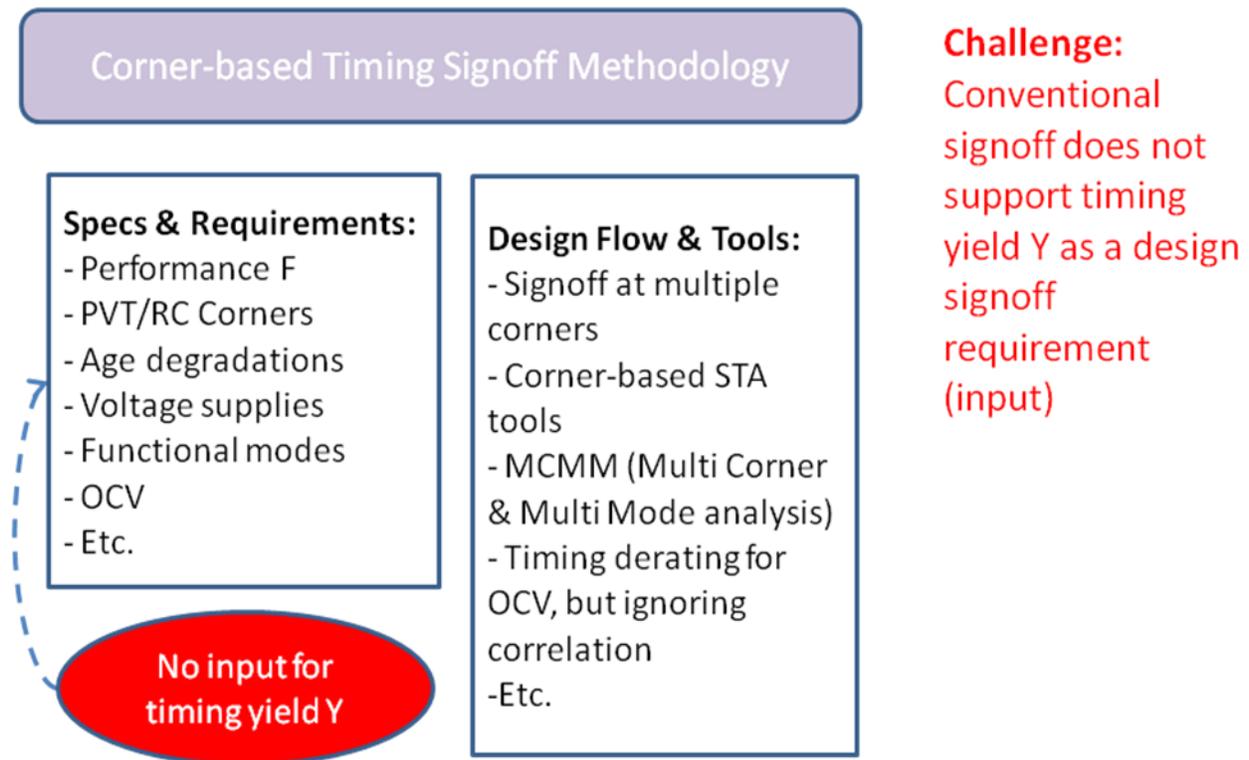


Figure 10 Corner-based signoff ignores the timing yield requirement

STA tools use timing derating (margins) to cover for different variations. Designers are using greater margins for each new technology node because there are more sources of variation and their magnitude increased. Larger margins have a significant impact on the maximum performance F that can be achieved for a technology node. Excessive and an unjustified margin increase for each next technology node leads to a significant lost in performance and over-design. The Figures below provide our estimate for the performance F and performance losses respectively, where all estimates are based on using the average increase of timing margins by ~1-2% for each next technology node).

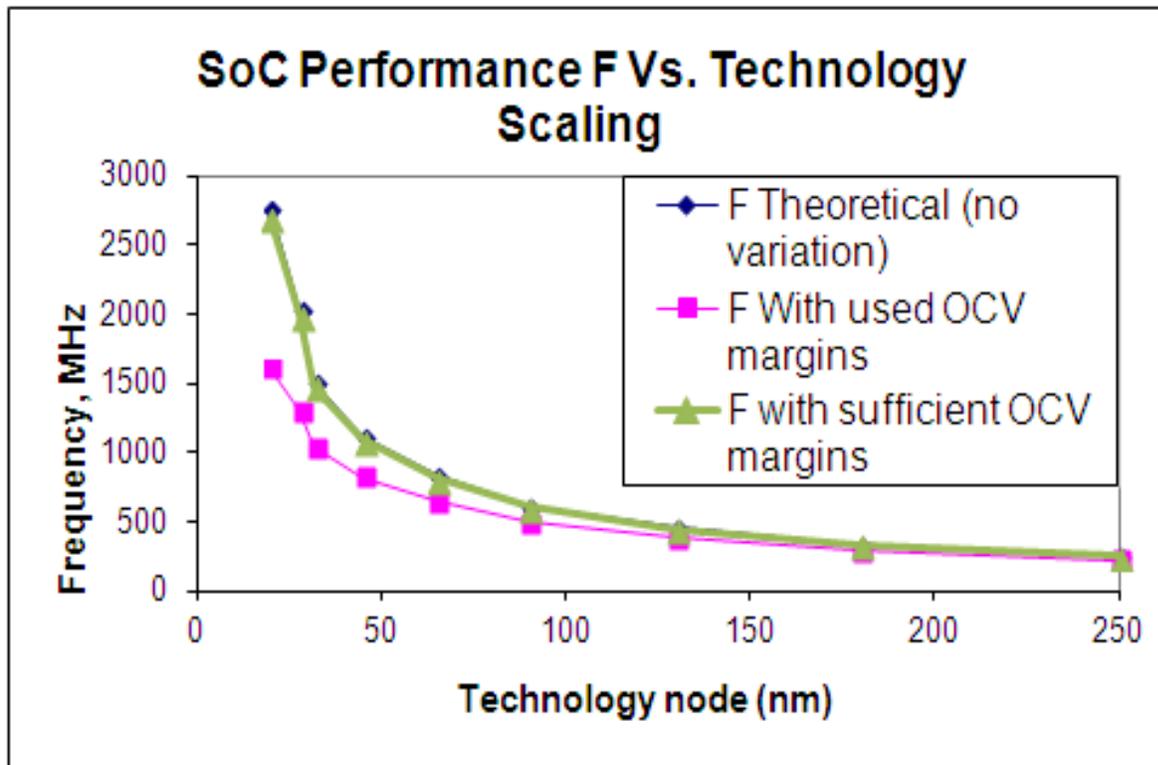


Figure 11 System performance is decreased due an excessive simplified derating

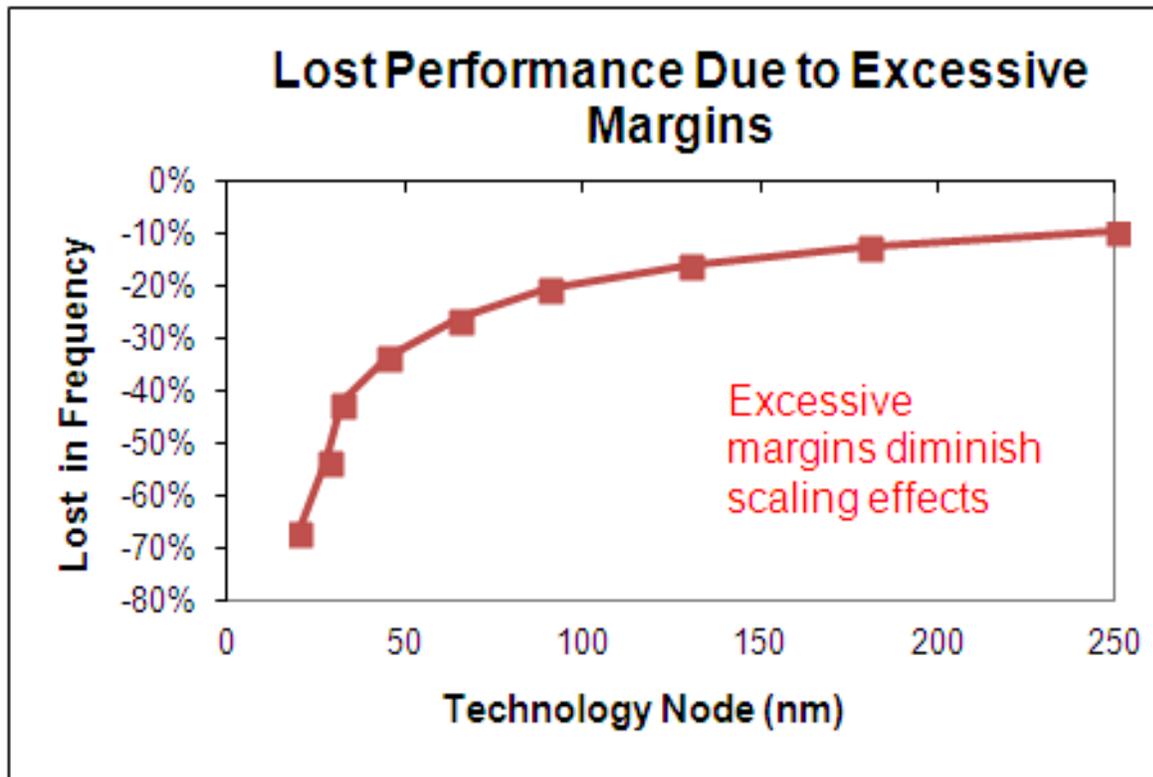


Figure 12 Lost in SoC performance due an excessive simplified derating

This lost in performance due to simplified and excessive derating has become a real challenge. Let's quote Jim Hogan of Vista Ventures [4]: *"During signoff, designers use multiple over-margining to pad against surprises in timing, clocks, power grids, yield, manufacturing variance, etc. Rule-of-thumb margining is over at 20nm: there is no longer enough margin. Gross percentage adjustments are also over: On Chip Variation (OCV) from the foundry can run as high as 20%, and when combined with padding for clocks, jitter, voltage, and local temps, it's impossible to close timing at all corners at your target power and speed."*

Thus, STA-based timing signoff methods:

- Use Corner-driven paradigm
- Are very important and accurate tools for calculating not-derated delays at a characterized corner
- Use OCV/AOCV approximate derating with several drawbacks [5, 12] that may increase a risk of a silicon failure and diminish design metrics (some of them will be discussed in details later)
- May become time-consuming due to ever increasing corner numbers and a rare occurrence of most corners:
 - Considering all conceivable corners and spending most time on analyzing very unlikely corners at the expense of a more accurate analysis of realistic and important corners
 - All paths are treated in the same manner and a lot of time is wasted on analyzing paths at corners where they never fail

- A few really vulnerable paths may be not analyzed at all needed and relevant corners for them
- Confidence level of timing is not consistent in different stages (of sub-paths or paths) and may be too conservative (up to the 10-sigma for typical stages: the probability of such case is $P \sim 10^{-23}$)
- Use the best-in-industry but still approximate and inaccurate timing derating methods (OCV, AOCV, LOCV, POCV, etc.) in commercial tools

Statistical STA (SSTA) timing signoff methods and tools use global corners paradigm too. These tools address some issues, but are not panacea. They:

- Are not truly statistical (rather approximate, not Monte Carlo based methods)
- Perform only a local variation analysis at a given global corner
- Take into account mainly transistor process variations, even though there are multiple other factors
- Handle the interconnect statically even though the interconnect delay variations may be comparable or even greater than the cell delay variations
- Ignore correlations or handle them simplistically
- Require a significant runtime and 10x disk space increase for libraries characterization

Concluding our brief discussion on current timing closure methods (STA/SSTA tools), we can state that they:

- Are state-of-the-art tools for the corner-based paradigm and not-derated delays
- Are a must in the current design flow and future possible enhancements
- May miss a failure in a few paths
- Have a lot of conservatism in the rest of paths
- May increase the TAT for fixing false issues at multiple corners and diminish some design quality metrics

Signoff Optimism and Conservatism (Pessimism)

Even though the conventional tools are conservative for most paths (as we mentioned above and will consider in detail below), there may be some optimism also for a few paths. This optimism constitutes a risk of a silicon failure. Possible optimism in timing is due to some limitations and drawbacks in contemporary timing derating methods [5, 12]. For example, derating tables assume some “bad” scenarios in paths. These scenarios are rare but still not the worst possible scenarios that may occur in real designs. It is a common industry approach to ignore really “worst scenarios” in a few paths in order to avoid too much conservatism (pessimism) for the rest (majority) of paths. Those few really worst paths (if any in the design) are still at risk because they may be optimistically estimated. Another reason for optimism is ignoring the number of critical paths.

Additionally, Place and Route tools do not separately balance cell and net delays in clocks. It may lead to problems. For example, Figure below shows a pictogram for a path with a “bad” structure: The launch and data paths are fully net delay dominated and the capture is fully cell delay dominated. Signoff at many not traditional PVT/RC/VRC corners and sufficiently big margins are needed to avoid a silicon failure if OCV/AOCV methods are used. Also, AOCV

derate tables cannot take into account an inter-clock correlation properly and it may lead to optimism too. There are also other OCV/AOCV limitations and drawbacks that may cause optimism [5, 12].

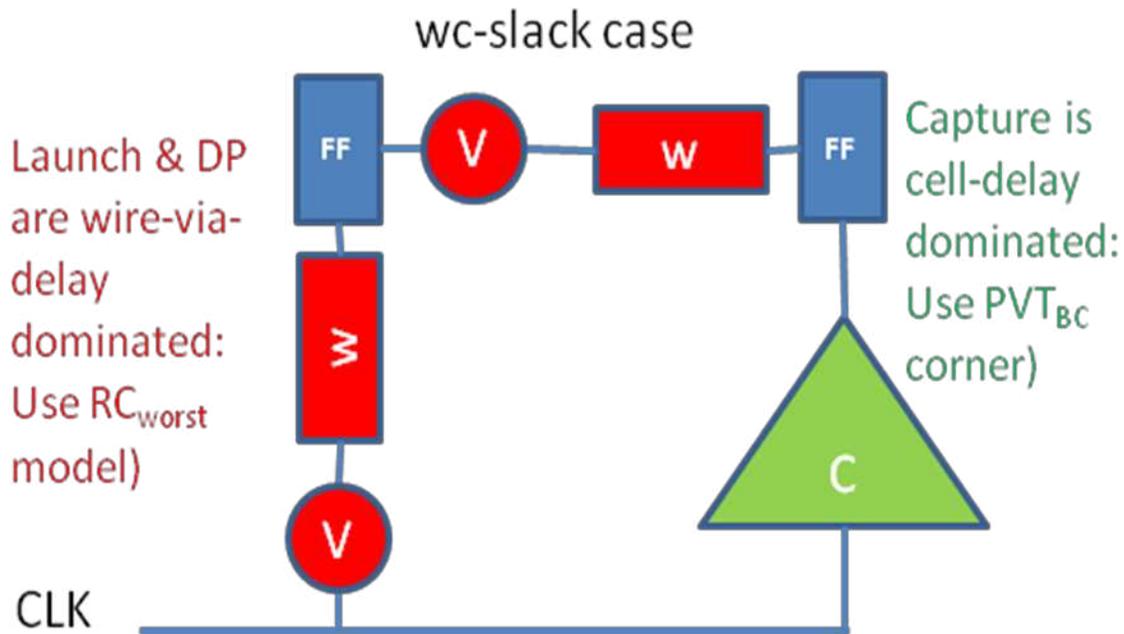


Figure 13 Illustration of possible optimism in timing

Figure below illustrates possible optimism in setup and hold check according to our study of 3 designs.

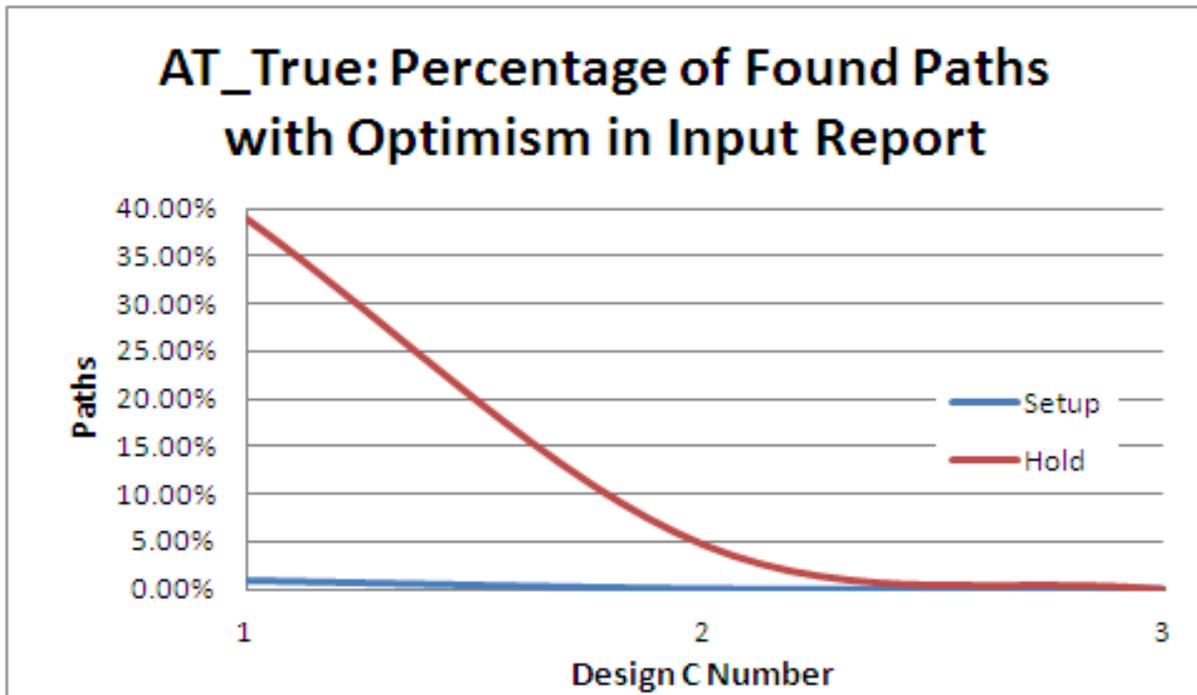


Figure 14 Illustration of possible optimism in timing

This study shows that:

- ~39% hold slacks were under-estimated in design C1: a relatively high risk factor
- ~1% paths with setup violations were overlooked in this design too

Hold violations are the most critical and must be never missed. OCV/AOCV timing margins (derates) are critical and must be relatively big to avoid hold catastrophic failure illustrated in Figure below. If one ignores EDA tools and libraries inaccuracies, then a risk of a failure increases because the tools are not modeling some analog effects in the digital logic (as an example) with the error on the timing up to $\pm 5\%$ and, thus, “... there will be hidden timing violations that will not be discovered until first silicon.” [3]. Note that foundries (like GlobalFoundry) validate quality of libraries and EDA tools, and foundry PDK before releasing reference design flows.

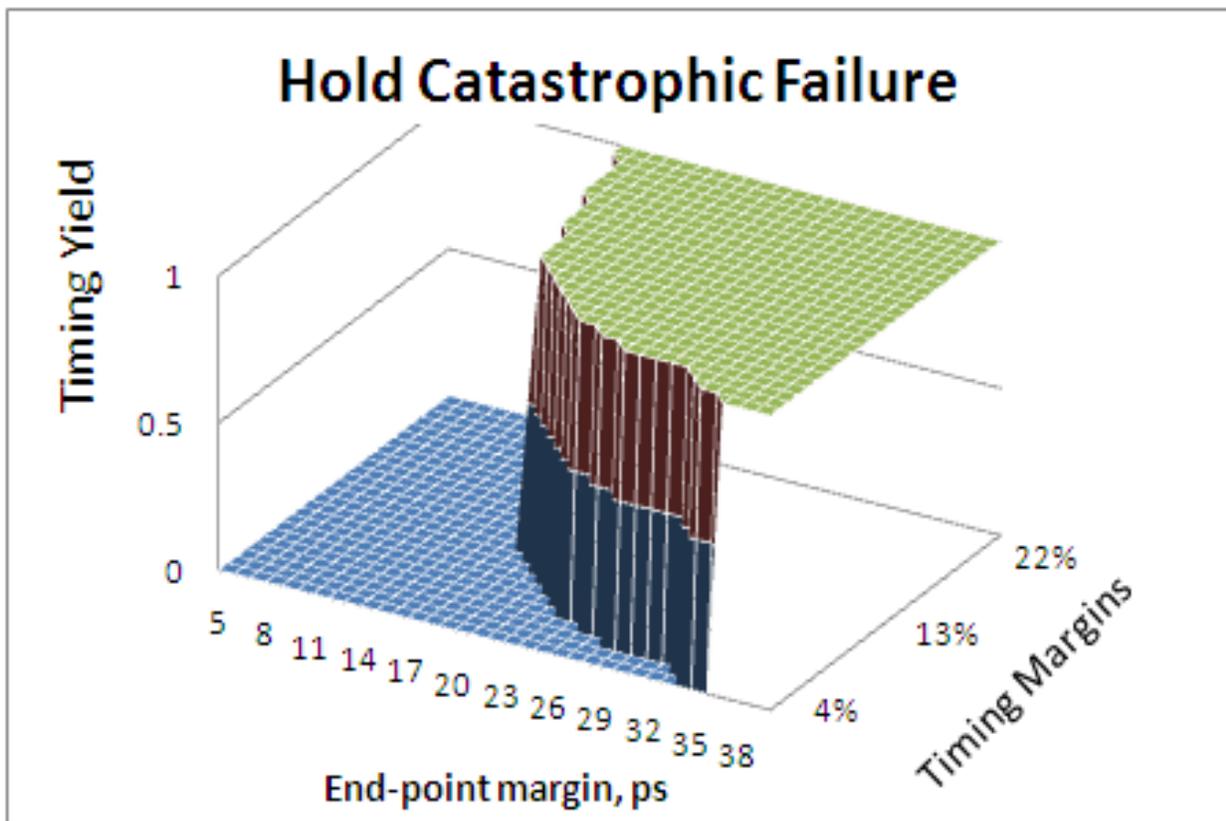


Figure 15 Illustration of hold timing yield vs. margins

Setup violations are also important and must be not underestimated because it leads to:

- Less timing yield
- Failure to meet spec performance F

Pessimism in conventional tools is due to:

- Using the extreme-corner definition and corner-case methodology: Corners and Derate Tables assume some “bad” but rare scenarios in paths and “typical” paths will be pessimistically estimated and over-designed
- Statically combining cell, wire and via corners

- Using unjustified conservative margins
- Statically adding a conservative (WC-scenario) crosstalk and the aging degradation
- Ignoring the internal path depth and build-in margin in complex cells
- Ignoring probabilities that paths are sensitized and that these probabilities are different and this impacts the timing yield in complex designs, which are increasing in a size, having more hierarchy, and getting more power-saving modes (like “on”, “off”, “sleep”, and clock/gating)
- Having several limitations, “safety” measures, assumptions that may not hold for some paths, and drawbacks in current conventional methods (AOCV, POCV, LOCV) even though that these methods are significant step ahead vs. the initial global OCV derating

Extreme global combinations of X-variation factors may happen very rarely: roughly $10^{-3 \cdot \text{Factors}}$. Currently the number of the most important X-Factors is ~ 10 (Factors=10 for our estimations). Thus, the probability P of an extreme corner is in a range of $[10^{-20}, 10^{-30}]$ and corresponds to a very rare situation. Note that we increased the lower bound due the fact that some X-factors have the uniform distribution law rather than Gauss.

Adding any new variation property (X-factor) leads to approximately a 10^{-3} decrease in the probability P of the extreme-case scenario of a new signoff corner for a typical path structure. An introduction of via points (models) is expected soon (according to our prediction). It will add ~ 4 new variation factors (like the via width, high, spacing, and dialectical thickness), then probability P will become even lower: $[10^{-30}, 10^{-40}]$. It will add even more conservatism on most paths.

The conventional ECO philosophy is: Fix all found violations across all corners/scenarios. This philosophy does not take into account a required (needed) timing yield Y_{REQ} . So, more corners/scenarios, more factors, more fixes are needed and it all leads to significant pessimism. Actually, there is no need to fix all violations to obtain the desirable yield Y_{REQ} . Thus, a challenge is that the number of corners and double-digit margins increase pessimism in timing and significantly reduce potential performance that can be achieved for each new advanced technology.

Variability Sources

There is an increased process variance both at the device level and on metal for each next technology node. Additionally, there are multiple sources of variations that must be taken into account. Conventional derating methods do not differentiate between sources of variation: All variations are combined into one margin value or table. Statistical STA (SSTA) tools mostly take into account local variations in the transistor process at one global corner. Numerous correlations are practically ignored or very simplified methods are used. Finally, there is a limited support in determination of derates [8].

Along with traditional variation sources like the PVT or RC, we need to include tools, libraries, and characterization’s inaccuracies [6]. It is just not possible to use the transistor/wire/via level of simulation in STA/SSTA tools due to complexity and the runtime. Thus, many electrical level effects are modeled approximately (not at a Spice level of accuracy). Note that Spice-based tools

are not 100% accurate too: They are ~1% accurate vs. silicon and, additionally, cannot model and take into account most of variation sources. Let's mention a few examples of analog factors that impact accuracy and which are not properly captured today in the existing conventional STA tools: *“Designers are now beginning to see numerous analog behaviors in digital circuitry—low voltage operation, IR variance, lock tree jitter, Miller capacitance, temperature, stack effects, multiple input switching and process variance -- that all fall outside of traditional digital delay and slack analysis. These analog behaviors can impact timing accuracy by 5% or more, raising serious questions as to what is actually passing or failing.”* [3]

Among new aspects of variations we need to consider Multi-Voltage Domains (V-domains) variations. Now designs often have uncorrelated V-domains and they may have any combinations of min/max voltages or intermediate values. Considering all V-combinations may be expensive and not supported automatically. Using timing derates to cover for these variations is risky and pessimistic. Synopsys developed the SMVA (Simultaneous Multi Voltage Analysis) [1] method that is very effective for completely uncorrelated domains, but it may be conservative due to the extreme-corner based philosophy that presumes: All V-domains will have their worst case voltages. Partially correlated V-domains are not supported and a proper addressing these issues is a new challenge.

Next new aspect (a variation source) is the Aging Degradation (AD). It increases cell delays during the microchip life time caused by Negative-bias Temperature Instability (NBTI), Hot Carrier Injection (HCI), Bias Temperature Instability (BTI) and Positive-bias Temperature Instability (PBTI) phenomena. Signoff without taking into account the AD introduces risk of:

- Setup violations before the chip's End-Of-Life (EOL) time
- Hold violations when
slowdown (happening during the chip's life time) in the capture is more than in the launch and data

Conventional tools do not directly support the AD. Additionally, e.g., at a slow corner it is not enough to derate up all delays or use the EOL libraries. There may be such path structures where setup violations happen at the Beginning-Of-Life (BOF)—and derating delays up will actually mask violations. Thus, taking into account the AD properly is a challenge for STA tool developers and designers.

Another variation source is Layout Dependent Effects (LDE) or Proximity Effects (PE):

- Well PE
- Stressors (STI, stress liners, embedded SiGe, etc.)

Handling correlations within variation sources and between sources is another challenge. Conventional tools use extreme scenarios to create worst- and best-cases for Data/Clock sub-paths and timing checks assuming (in order to simplify estimations):

- 100% correlation within each sub-path
- 0% correlation between sub-paths

It results, for example, that current tools do not provide direct support on correlations between clocks in the AOCV derate tables. Tables take into account clock distances only. During an AOCV table generation, if we assume [8]:

- Worst case of clocks location, it will lead to pessimism
- Best case of clocks location, it will lead to optimism

There is no way now to describe distance between clocks and provide inter-clock derate tables.

Crosstalk effect is also a variation source, but it has a dynamic nature. Conventional tools assume the WC signal alignment for all victims and aggressors in all stages of sub-paths. It leads to pessimistic estimates for many paths, because such WC scenario may occur very rarely (once in 1, 2 ... or more years of the chip life time). Static handling crosstalk ignores factors such as the Time-To-Failure (TTF), design frequency F, the number of paths with crosstalk and realistic probabilities of crosstalk impact. Current methods are pessimistic in several paths as a result. Handling crosstalk and other dynamic variations is an important challenge too.

In conclusion, the above described variations impact accuracy of conventional tools that use a timing derating to model variations. Accuracy may be not high enough if paths' structures/properties differ from the method's assumptions. Accuracy of the derating becomes an issue due to increased number of variation sources and their magnitude. *"More than 40% of the delay through the cell can be attributable to local or on-die variance. This increases the spread between corners, and requires larger derates (OCV or AOCV)"* [3]. Ignoring some variation sources and inaccuracies in modeling variations may lead to:

- Optimism in timing (a risk factor) and even to a silicon failure
- Pessimism that worsens all design metrics

Timing Signoff Deadlock

Let's now outline main contemporary issues in closing timing:

- Closing timing becomes more and more difficult for each next technology node:
 - Designers must close timing at numerous extremely rare corners and the number of corners grows. *"It is becoming almost impossible to close timing in all corners, given the ambitious (and often conflicting) specs for power and frequency, process variance, corner spread, large derates..."* [3]
- The difference in delays (the delay spread) at different corners is becoming greater for each next node. *"The spread between each of the corners is very large due to die-to-die process variability on metal and device. So even if the number of corners is reduced, it does not eliminate the designer's problem of having to satisfy timing in all possible scenarios. These large on-die variabilities (local variance) result in very large OCV and AOCV derate factors. This makes it harder to close timing even in any one corner."* [3]

- The number of variation sources and their magnitude are increasing and demand more and more timing margins
- Inaccuracies require even more corners and margins

The above issues lead to multiple difficulties to fix violations. For example, designers can see setup violations at fast corners and hold violations at slow corners due to:

- Delay spread between corners
- Different sub-path structures (cell-, wire-, via-delay domination in clock and data paths; or any combinations of them)
- Increase in wire and via delays when these delays are becoming comparable or even greater than cell delays
- Other new physical phenomena mentioned above

Another example—Fixing a timing failure in a path at one corner may introduce a new violation at other corner(s). E.g.:

- Fixing a setup violation at a slow corner may create a hold violation at a fast corner
- Fixing a hold violation at fast corner may create a setup violation at a slow corner
- Vice versa situations are also possible

Figure below is an illustration for one particular situation of the deadlock for path P:

- There is a Setup violation for path P at WC corner ($\Delta T = T_L - T_C > T_{clk}$, where T_L is launch clock path delay, T_C is capture clock path delay, and T_{clk} is the clock period)
- There is no hold violation for P at BC corner: $\Delta T > 0$
- Fixing setup@WC leads to new hold violation for P at BC corner
- Factors leading to deadlock:
 - Higher F: Setup/hold timing window ($=T_{clk}$) becomes smaller
 - $T_{wire} \approx T_{cell}$ & T_{via} grows: more diversity in path delays combinations & higher probability of some “bad” structures (combinations)
 - Increased OCV/AOCV derates
 - Inaccurate derating methods used in OCV/AOCV/POCV derating methods

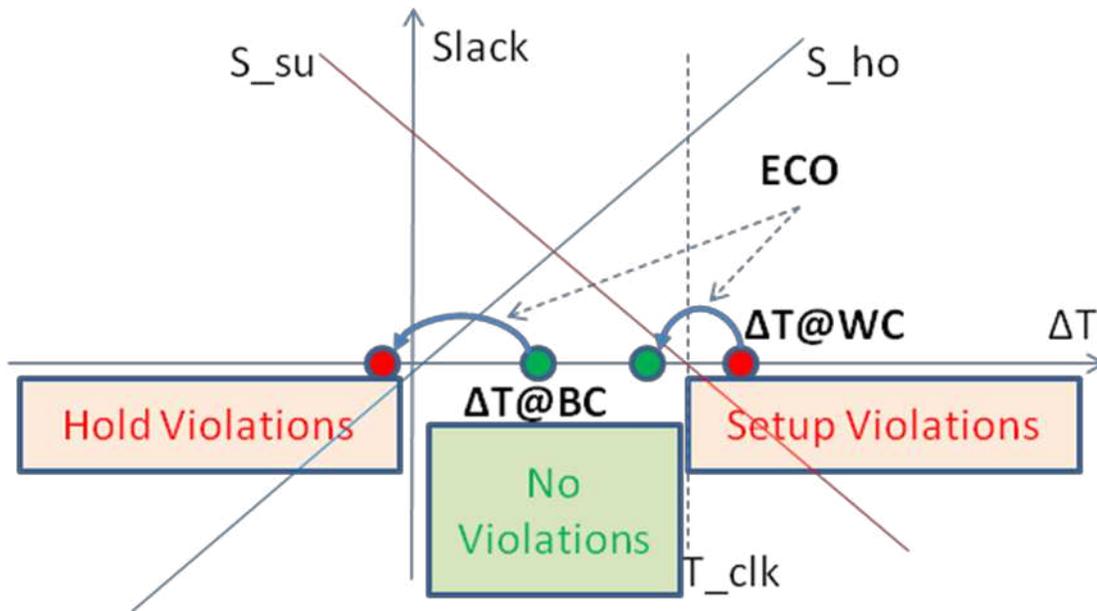


Figure 16 Illustration of possible signoff deadlock

The current STA/SSTA signoff methodology for digital systems is based on using multiple extreme corners. It has the following main drawbacks (and some of them have already been mentioned during corner number discussion above):

- Each corner is an extreme combination of cell, wire, and via variation scenarios of multiple X-factors (variation sources) what makes each corner pessimistic for a typical path structure
- Each corner has a very small probability to occur, but violations must be fixed anyway what is worsening all design metrics
- A typical stage will be estimated pessimistically using these rare corners what leads to over-design
- Multiple corners (up to 126 or even more) may be required for timing signoff what significantly increases the TAT and costs
- Several variation sources and correlations are not captured by conventional tools
- Timing derating methods (OCV, AOCV, LOCV, POCV) of contemporary STA tools have limitations that may lead to inaccuracy, pessimism and even a silicon failure risk

The described above difficulties to close timing is called the **timing signoff deadlock**. As a result, designers may need to:

- Sacrifice the SoC performance
- Incur a longer TTM and higher costs
- Take a risk to waive some violations
- Accept losses in the timing yield
- Get losses in quality metrics (like power, area, time-to-failure, etc.)

The signoff deadlock is mostly caused by an increased corner number and timing derates. Avoiding the signoff deadlock is almost impossible as long as the industry continues to use the corner-based signoff. This becomes a main challenge.

4. Advanced Timing Signoff Methods

Let's outline and, then, discuss possible enhancements in signoff paradigms, methods, and tools. We see 4 options that may be adopted by the industry:

1. Enhancing the AOCV derating method
2. Switching to the Parametric OCV (POCV)
3. Developing pseudo-statistical tools
4. Developing statistical Monte Carlo-based tools

Options (1) and (2) may be combined with minimizing the corner number and a detailed examination of variations in found risky (timing critical) paths. Possible methods may include:

- Using PrimeTime-SI (PT-SI) and running risky paths through multiple additional corners with a proper AOCV/POCV derating. There may be 100s of additional corners that may be based on all characterized libraries, all RC-extractions including DPT (and via models in the future), AD models, etc. This is computationally possible due to a relatively small number of risky paths.
- Using PrimeTime-VX (PT-VX) and running risky paths through multiple additional corners

Options (1), (2) and partially (3) may be considered if a company is using the corner-based signoff and this is a must-to-use method for the company no matter what it takes. Options (3) and (4) may be more beneficial as we will show below.

Option 1 (Enhancing the AOCV derating method) is developing and introducing some enhancements to overcome current limitations and drawbacks of the AOCV method. We call a new derating method as **EAOCV** (Enhanced AOCV or **AT-RITE** Abelite tool). The need for the EAOCV is due to the following AOCV limitations:

- Presence of sub-paths with not-uniformly distributed stage delays. In this case, the pre-defined derate tables provide optimistic derates.
- Simplified combining delay variations in cells, wires and vias in one derate value what is pessimistic because these variations are not correlated
- Ignoring:
 - Correlations within and between variation X-factors and between cells, wires and vias
 - Number of timing critical paths—the more such paths, the greater derating needed
- Handling crosstalk and some other dynamic effects in a conservative static way
- Handling the DPT in a conservative static way

- Simplified or not-justified methods of finding margins (and there is no serious support from the foundries and EDA vendors)
- Using the same derating tables for:
 - Setup and hold checks to minimize runtime (there are usually no separate STA runs for setup and hold)
 - Different PVT and RC/Via corners (it’s an usual case due to challenges in finding and supporting multiple derate tables)
- Presence of complex or hierarchical cells with:
 - Internal sub-paths with different path depths more than one
 - Internal built-in OCV margins

Some of the above issues can be enhanced or improved within the AOCV derating, but not all of them. This naturally leads to considering Option 2: Switching to the Parametric OCV (POCV). The POCV (Synopsys roadmap) derating can handle paths with not-uniformly distributed stage delays. It is more “statistical” by the way it calculates sub-path variations. Actually, we need to use term “pseudo-statistical” as a more accurate term for this method, because the only truly statistical method is Monte Carlo-based method, not “formula-based” methods like the RSS.

The POCV method is simpler for using—only one stage variation property needed to be provided by the user vs. derate AOCV tables with multiple entries. Still the POCV has its own limitations and drawbacks. Examples of limitations/drawbacks are:

- Static combining delay variations in cells, wires and vias
- Ignoring:
 - Correlations
 - Number of timing critical paths
- Handling crosstalk and some other dynamic effects in a conservative static way
- Possible accuracy issues due to using pseudo-statistical methods and other simplifications

Now, let’s move to Option 3: Developing Pseudo-Statistical Tools. We will call these methods **PS-STA** (Pseudo-Statistical STA or **AT-TRUE** Abelite tool). These methods will be based on using new paradigms. Namely:

1st Paradigm: Path-driven signoff:

- Corners are auto-selected for each timing critical path. AT-TRUE considers a path structure (all sub-paths, factors & values) & finds all corners where the path may potentially have violations. Even though there are 100s of different corners, each particular path needs to be checked at only a few (usually less 10) individual corners.
- Obtaining high accuracy of all timing estimations by using advanced pseudo-statistical methods that statistically sum stage cell, wire & via delay variations for each critical path. These methods take into account all variation objects, all variation X-factors & all correlations.

2nd Paradigm: **Stage-based signoff:**

- Equalizing risk at individual stages & paths by estimating an individual corner confidence level C for each stage/path & adjusting derating to have the same required confidence level K in all stages/paths

3rd Paradigm: **Delay Scaling To Corner:**

- Automatic delay scaling of cell, wire & via delays to all needed extreme corners to find all potential violators
- Using the minimal number of corners to be run through a conventional STA—only one nominal corner in most cases
- Optional using PrimeTime for the final signoff for all found violators at their corresponding corners (reported)

Let's outline must-to-have new features for PS-STA tools:

- Using pseudo-statistical (not MC-based) methods for timing derating. It means implementing a pseudo-statistical summation of stage delay variations vs. simple summing in conventional STA tools.
- Explicitly separating cells, wires and vias variations. It means using a pseudo-statistical summation for cell, wire and via variations vs. conventional STA/SSTA tools that ignore wire/via variations.
- Taking into account all sources of global and local variations in:
 - Transistor process including FinFET
 - Voltage (supply, static, and dynamic) in V-domains
 - Temperature in cells (including T-inversion), wires and vias
 - Geometry properties in wires and vias such as Width, Height and Dielectric Thickness and Double Pattern Technology (DPT) that varies wire spacing
 - Inaccuracies in EDA tools (like Extraction, 3D FinFET, Delay Calculation) and Libraries vs. Silicon
 - Dynamic crosstalk delay variations [9]
 - Aging degradation, etc.
- Powerful delay scaling to any PVT/RC/Via/AD corner
- Using new models that describe wire/via variations as functions of geometry properties and temperature
- Considering correlations. It means characterizing, modeling and taking into account correlations within and between X-variation factors. Ignoring correlated variations leads to timing inaccuracy. It is important to estimate correlations as functions of distance between different objects and their location. Additionally, it is important to consider correlations due to the same or different cell types or wire/via types (width, layers, directions, and sizes).
- Modeling cell, wire and via delay variations induced by the same correlated factor (like temperature T)

- Considering tools/libraries/flow inaccuracies as a type of variations and incorporating them into the derating to prevent optimism in timing
 - Inaccuracies (errors) may be pure random, correlated, centered or not-centered and have not the normal distribution
 - Tools, data, methodology and design flows are not perfect
 - Signoff tools (like Extraction, Spice, STA, SSTA, etc.) and Libraries are not 100% accurate
 - These inaccuracies are significant
 - Ignoring these inaccuracies is a risk factor
- Taking into account the number N_{CR} of timing critical paths that may require an increased confidence level up to ~ 4.5 sigma to avoid optimism
- Achieving a requested (by the user) confidence level (like 3-sigma) for the whole design:
 - Not just for one stage or path
 - Matching a corner confidence to an individual stage situation: typical stage does not need a 5-10 sigma confidence
 - This confidence level is a function of N_{CR}
 - If design has more critical paths, the timing yield is decreasing and the silicon failure risk is increasing because a violation only in one path may cause a die failure

We may conclude that PS-STA will be a pseudo-statistical tool with path-individual corners, advanced delay scaling, handling multiple variations sources and correlations. This approach allows using the minimal number of corners (or even only one nominal corner) with follow up automatic delay scaling of cell, wire and via delays to all needed extreme corners to find all potential violators. The final signoff may be performed by PrimeTime for all found violators at their corners. Main limitations and drawbacks are due a pseudo-statistical approach that does not allow to estimate the timing yield, may be not accurate enough (especially at scaled corners), demands fixing all found violations at all corners, and still requires to finally run PT-SI for found violations.

As we described above, PS-STA have their limitations and drawbacks. This justifies a need to develop truly statistical methods based on Monte Carlo (MC) analysis. So, let's finally consider Option 4: Developing statistical Monte Carlo-based Tools. We will call these methods **MCS-STA** (Monte Carlo SSTA or **AT-STAT** Abelite tool). These methods will be based on using new paradigms. Namely:

1st Paradigm: Variation Space-driven Signoff:

- Accomplishing timing signoff at the whole variation space (thousands of points) vs. the current corner-based paradigm

2nd Paradigm: Timing Yield-driven Signoff:

- Finding timing yield, statistical slacks & timing derating across the whole variation space vs. the fixed number of extreme corners

- Using a new definition of a path/design failure—not each path with negative slack at some point is a violator & leads to a silicon failure

3rd Paradigm: **Yield-based Violations Fix:**

- Fixing the minimum number of violations to obtain a requested timing yield

Note that in this signoff method we replace Corners with Points:

- Variation space point (Point) is a combination of global X-factor values, which may be not extreme values
- Points are used instead of Corners
- There are much more Points than Corners
- Corners are Points too (Points with extreme values)
- Points are distributed properly in the variation space corresponding to the distribution laws for X-factors
- Point is a combination of global X-values for all die guys plus local (OCV) variations of X-values for each guy (cell, wire, and via) in the chip. OCV are additional changes of X-factors corresponding local changes for each cell/wire/via and each X-factor.
- Nominal Corner corresponds to Nominal Space Point and is the main Input Corner

Let's outline must-to-have new features for MCS-STA tools:

- Using a Monte Carlo-based statistical engine
- Having all new features listed (above) for PS-STA tools
- Finding all real timing violations is a must
- Minimizing pessimism is a crucial task that improves Performance, the TAT, Costs and Design metrics
- Finding and fixing real timing violations (not just paths with Slack<0):
 - Some violations may not mean zero or an unacceptable timing yield Y
 - Path criticality and estimated timing yield Y for the design across all points must be taken into account to make decision if the violation must be fixed or not
 - It minimizes the TTM and design cost
- Using voltage and temperature local variation maps (if known)
- Statistical estimating of DC/AC/Total power consumption
- Handling partially correlated (derived) voltage domains (supplies)
- Obtaining timing derating close to silicon delay variations by using a correct-by-construction MC method

Note that implementing a MC-based full-blown variation space engine is a very challenging task. Its goals and challenges are obtaining the highest accuracy possible and modeling all effects while having an acceptable runtime and minimal characterization costs for all variation sources. To solve these challenges one can use such approaches as considering (finding with using contemporary STA tools) only timing critical paths; using a state-of-the-art MC-based statistical engines with additional covering of possible computational errors caused by generating a reasonable (but relatively small) number of samples; developing a highly effective delay scaling in the

multi-dimensional PVT/RC/Via/AD space; obtaining acceptable accurate delays in peripheral arias of the variation space based on an approximate characterization of variation sources; and using parallel statistical engines.

Figure below shows a comparison between the above described emerging advanced signoff methods.

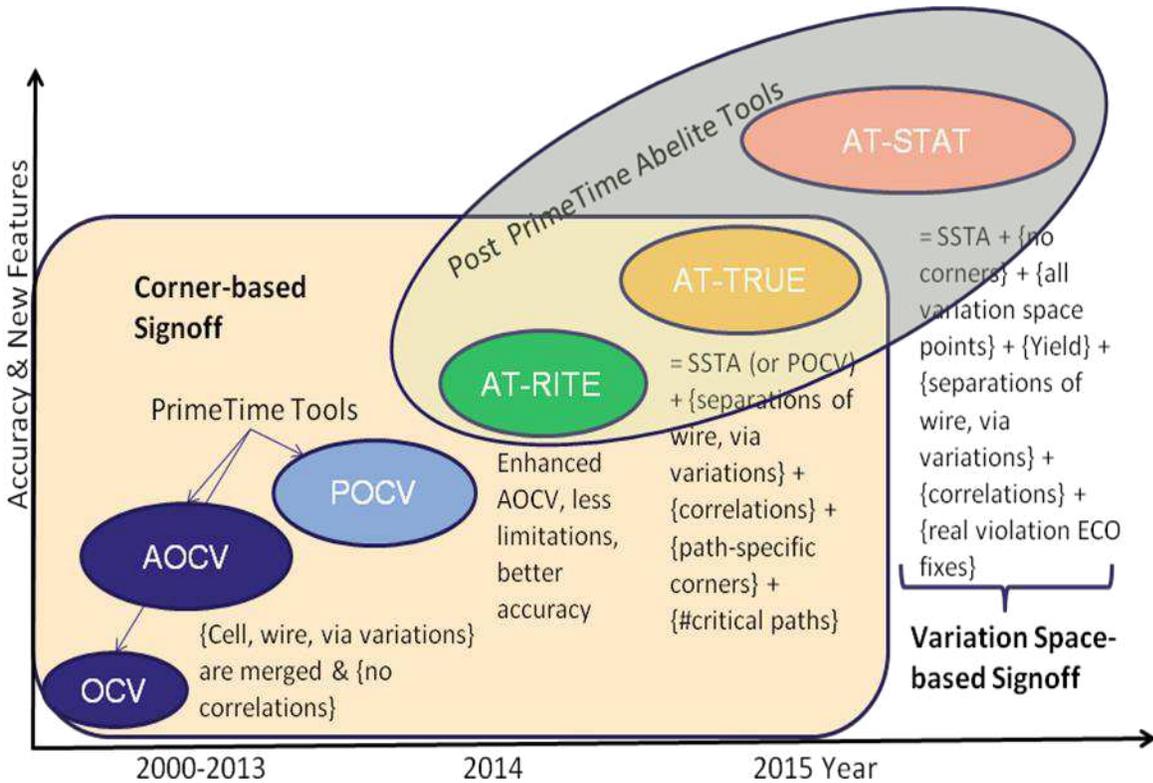


Figure 17 Signoff methods comparison

Finally, after analyzing PS-STA and MCS-STA methods we have to conclude that they are computationally expensive, especially the MCS-STA. It is not likely they will replace the AOCV/POCV in PrimeTime (PT) and ICC. They can be used on top of PrimeTime (namely, after a PT run):

- PT is a state of the art tool with trustable timing especially for Nominal Corner (NC)
- PT is recommended to obtain a golden timing for NC
- PT can be used to find all potential violations
- New advanced tools can be run as post-processing tools to make timing derating more accurate, to find the timing yield and violations to be fixed
- Parallel execution may be important

Finally let's discuss how one can validate these new methods and tools:

- New tools are not possible to validate using Spice because Spice cannot:
 - Take into account all variation sources
 - Take into account correlations
 - Handle real designs (their sizes)
 - Estimate the timing yield
- They can be validated using real silicon [10] or other test-chips. This is recommended for each new technology, but it may be objectionable for any production design due to the cost and TTM considerations
- If the tool is Monte Carlo based, then it is correct by construction (excluding bugs)
- Also, new tools will re-use golden PrimeTime delays (without derating) and the only difference is in timing derating. Having several new tools (EAOCV, POCV, PS-STA and MCS-STA) will allow increase confidence in correct derating.

5. Conclusions

The paper shared our experience and knowledge on signoff methods and calls for developing new post-STA tools to implement new signoff methodologies. Additionally, PrimeTime users can obtain all Abelite's tools/scripts, which are complementary to Synopsys best-in-class tools/flow [3, 4].

We hope we have accomplished our main goals:

- Raise awareness about timing signoff challenges & drawbacks of commercial tools and signoff methodology
- Outline roadmap for new timing signoff methodologies and tools
- Provide brief information about Abelite new released and emerging methods/tools

In conclusion, let's try to outline an emerging advanced signoff philosophy:

- Design resources and time are limited and must be spent on timing critical paths:
 - If designers are fixing “false violations”, it makes more difficult to fix real problems or improve design metrics
- Performing timing signoff at the whole variation space rather than at multiple rare extreme corners
- Taking into account all variations and errors including:
 - EDA tools/libraries inaccuracies
 - Global and local variations
 - Wire geometry and temperature
 - Via geometry and temperature
 - Dynamic crosstalk, etc.
- Handling complex correlations
- Using new pseudo-statistical and truly statistical Monte Carlo methods
- Handling timing yield and confidence level requirements

- Validating timing results [10]

And finally, below we provide a summary of this paper:

- Timing signoff experts know statistics on:
 - Number of designs that were not closed at a spec frequency in spite of all the design efforts and time
 - Number of re-spins for designs due to an insufficient timing yield or a silicon failure
- These statistics are not published and the reasons are understandable. This is happening in spite of all the advancements in technology, EDA tools and methodology developed at Semiconductors, EDA and Electronics industries
- New advanced tools are emerging because:
 - There is no room for a silicon failure
 - More accurate timing is needed to avoid pessimism
- These tools improve accuracy, provide risk management, minimize pessimism and the signoff corners number
- Emerging technologies are based on new paradigms to advance timing analysis and solve the contemporary challenges

6. References

- [1] HOGAN, Jim (Vista Ventures): <http://www.deepchip.com/items/0524-04.html>
- [2] KATZ, Isadore, CLK-DA Inc: <http://www.deepchip.com/items/0534-03.html>
- [3] Synopsys PrimeTime Advanced Timing Analysis User Guide: https://solvnet.synopsys.com/dow_retrieve/E-2010.12/ptuga/ptuga.html
- [4] IC Compiler 2010.03 Update Training: <https://solvnet.synopsys.com/retrieve/030453.html>
- [5] 16 OCV Myths: <http://abelite-da.com/address/myths-about-global-variations/>
- [6] PVT/RC/Via Corners: <http://abelite-da.com/address/pvtrc-corners/>
- [7] WU, S.H., TETELBAUM, A., WANG, L.C. “How Does Inversed Temperature Dependence Affect Timing Sign-off”, in Proc. of 2007 International Conf. on Integrated Circuits Design and Technology, Minatéc Grenoble, France, June 2nd – June 4th, 2008, pp. 297-300.
- [8] TETELBAUM, A., LAUBHAN, R., KEYSER, D. Advanced OCV Timing Derating Experience, In the Proc. of the SNUG Conference, San Jose, 2011, 19pp.
- [9] TETELBAUM, A. “Statistical STA: Crosstalk Aspect”, in Proc. of 2007 International Conf. on Integrated Circuits Design and Technology, Austin, Texas, USA, May-June, 2007, pp. 27-32.
- [10] VENKATRAMAN, R., TETELBAUM, A., CASTAGNETTI, R. " Experimental Methodology for Validating Timing Closure with Advanced On-Chip Variation (AOCV) ", in Proc. of DAC'11, San Diego, USA, June 2011, pp.688-693.
- [11] High-Sigma Monte Carlo (white paper): <http://www.solidodesign.com/page/hig...memory-design/>
- [12] TETELBAUM, A. “Abelite Advanced Timing vs. STA & SSTA Tools”: http://abelite-da.com/wp-content/uploads/2014/01/Abelite_vs_STA_SSTA.pdf