The High Speed SERDES IP Company
Corporate Overview

• Founded in 2012 by a team of senior analog designers who worked together at TI for many years.
• Main Expertise: Analog design & integration into large SOCs.
• Company Products:
  • High Speed Serial Interfaces IPs (SERDES), Low jitter PLLs and I/Os.
  • High Speed ADC/DAC
  • SERDES Digital Controller for JESD204B and other standards
• Silicon Proven: Successfully taped out several SERDES IPs.
• Design Centers in Bangalore (analog & digital design) and Pune (IP Verification).
• Total team of 40 engineers.
• Well equipped lab capable of characterizing high speed SERDES IP and running compliance tests.
• Company is privately held
SilabTech Portfolio

High Speed SERDES IP
- **12.5 Gbps Multi Standard SERDES**
  - PCIe3, USB3.0/3.1, SATA, XUAI, RAPIDI/O, HMC, VbyOne, HSSTP
  - 10G BASE KR, DisplayPort
- **MIPI SERDES**
  - DPHY; MPHY; C+D Combo PHY
- **JEDEC JESD204B**
  - SERDES & Controller
  - 0.3 – 12.5 Gbps

Analog IP
- **ADC & DAC**
  - 8bit / 3.5 Ghz
  - 10bit / 500Mhz
  - 14bit / 250Mhz
- **Low Jitter PLL**
  - 0.1 to 8 Ghz

Services
- **Complete Chip Design**
- **IP Sub-system Integration**
- **SERDES migration to Proprietary & Legacy processes**
## SERDES IP - Silicon History

<table>
<thead>
<tr>
<th>Speed</th>
<th>Standards</th>
<th>Process Node</th>
<th>Status</th>
<th>Silicon status</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.25 Gbps</td>
<td>Multi-standard 1-6.25 Gbps</td>
<td>GF 28 SLP</td>
<td>Silicon</td>
<td>First pass success. Data available</td>
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<td>6 Gbps</td>
<td>MPHY HS Gear 1/2/3</td>
<td>GF 28 SLP</td>
<td>Silicon</td>
<td>First pass success. Data available</td>
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<td>12.5 Gbps</td>
<td>Multi-standard 1-12.5 Gbps Short Reach</td>
<td>TSMC 28HPM</td>
<td>Silicon</td>
<td>First pass success. Data available</td>
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<tr>
<td>12.5 Gbps</td>
<td>Multi-standard 1-12.5 Gbps Long Reach</td>
<td>SMIC 40 LL</td>
<td>Silicon</td>
<td>First pass success. Data available</td>
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<tr>
<td>6 Gbps</td>
<td>Custom design for tier 1 customer</td>
<td>TSMC 28HPM</td>
<td>Silicon</td>
<td>First pass. Data is customer proprietary</td>
</tr>
</tbody>
</table>
Data Converters ADC & DAC

**Analog to Digital Converter (ADC)**
- 8 bit / 3.52 Ghz
- Based on interleaved SAR architecture
- Each SAR ADC is 8bit/ 440MHz
- 8 ADC’s are interleaved to achieve 3.52GHz data/sampling rate
- GF 40LP- Silicon Results by Nov-15

**Digital to Analog Converter (DAC)**
- 8 bit / 3.52 Ghz
- 8-bit Differential Current Steering DAC is based on 1.1V supply.
- 50 ohms Differential Termination
- Output voltage swing of 500mVpp differential (programmable 400->600mV)
- Different Input data rates are re-align internally, e.g. 64 bit data at 440MHz or 32 bit at 880MHz.

**Product Roadmap:**
- 10bit / 500 Mhz SAR ADC  TSMC 65nm
- 12bit / 250 Mhz Pipeline ADC  GF 28SLP
- Multiple ADCs and JESD204B SERDES ASIC
Analog Design and QA Flow

CIRCUIT DESIGN AND LAYOUT
- Schematic design with estimated parasitics (including package)
- Simulation for block level specs
- Analog layout and parasitics extraction
- Post layout simulation (back-annotation with extracted parasitics)

FUNCTIONAL INTEGRATION
- Verilog/VHDL modeling of analog
- Verification of digital design with analog model
- Gate level simulations with timing model of analog
- Co-simulation of digital (HDL) and analog (SPICE)

PHYSICAL INTEGRATION
- Package requirements
- Package design/extraction
- Signal integrity/power integrity simulations
- PCB design/extraction
- Signal integrity simulations

IP electrical spec verification & design review
IP functional verification
IP functional & performance verification
IP functional verification. Limited performance verification
IP electrical spec verification
Eye Diagram at 12.5Gbps TSMC 28 HPC

Data rate = 12.288Gbps (UI=81.4ps)
Far-end eye diagram at the end of a short reach channel
Data pattern: PRBS15

TSMC 28HPM
Results from 1st silicon in this technology
Far-end Eye Diagram at 6.25 Gbps

Data rate = 6.144Gbps (UI=162.8ps)
Far-end eye diagram at the end of a short reach channel
Data pattern: PRBS15

TSMC 28HPM
Results from 1st silicon in this technology
Silicon Results (RX)

TSMC 28HPM

UI: 80ps (12.5Gbps)
DATA: PRBS7
SWING: 600mV pp
# SERDES – Supported Standards

<table>
<thead>
<tr>
<th>Application</th>
<th>Standards</th>
<th>Data Rate Per Lane (Gbps)</th>
<th>Standard Organization</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PC/Server</strong></td>
<td>USB 3.0 / 3.1</td>
<td>5 / 10</td>
<td>USB Forum</td>
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<tr>
<td></td>
<td>PCIe Gen 1/2/3/4</td>
<td>2.5 / 5 / 8 / 16</td>
<td>PCI-SIG</td>
</tr>
<tr>
<td><strong>Mobile</strong></td>
<td>C-PHY, D-PHY, M-PHY</td>
<td>1.5 / 2.5 / 5.8</td>
<td>MIPI.ORG</td>
</tr>
<tr>
<td><strong>Storage Devices</strong></td>
<td>SATA Gen 1/2/3</td>
<td>1.5 / 3 / 6</td>
<td>SATA</td>
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<td></td>
<td>HMC- Hybrid Mem Cube</td>
<td>12.5</td>
<td>HMC Forum</td>
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<tr>
<td><strong>Data Networks</strong></td>
<td>1000Base-KX</td>
<td>1.25</td>
<td>IEEE</td>
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<td>XAUI</td>
<td>3.125</td>
<td>IEEE</td>
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<td></td>
<td>CEI-11G-SR/LR</td>
<td>9.95-11.1</td>
<td>OIF Forum</td>
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<tr>
<td></td>
<td>SGMII/ QSGMII</td>
<td>1.25 / 5.0</td>
<td>CISCO</td>
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<tr>
<td><strong>RF</strong></td>
<td>JESD204B</td>
<td>1.25 – 12.5</td>
<td>JEDEC</td>
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<td></td>
<td>CPRI</td>
<td>9.8304</td>
<td>CPRI Forum</td>
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<tr>
<td><strong>Debug</strong></td>
<td>HSSTP - High Speed Serial</td>
<td>1-12.5</td>
<td>ARM</td>
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<td></td>
<td>Transmit Port</td>
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<tr>
<td><strong>Display</strong></td>
<td>Video-By-One</td>
<td>4</td>
<td>Thine Elec.</td>
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<tr>
<td></td>
<td>DisplayPort</td>
<td>1.62 / 2.7/5.4 / 8.1</td>
<td>VESA</td>
</tr>
</tbody>
</table>
Unique Advantages

- Silicon Proven IP Cores- SERDES, ADC, PLL and other Building Blocks
- Solution Level for complete Interface- SERDES and Controller
- Industry’s Lowest Power figures – 30% lower power!
- Flexibility and Customization are all possible- Focus on customer needs
- Experience in building large SOCs & ASICs and not just IPs.
- Unique large services team supporting IP integration to target SOC.
- Top quality design from a company with low design overheads.
- No 3rd party restrictions on any IPs or designs.
Thank You

Contact us on sales@silabtech.com

www.SilabTech.com