Esencia Technologies

Excellence in FPGA & ASIC Implementation

BEST IN SHOW WINNERS

Best in Show
Chip Design: GUC

Best in Show
Software: Esencia Technologies

Best in Show
Hardware: Qualcomm & Intrinsyc Software International

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Profile

Team

- 90+ Engineers in Silicon Valley (Santa Clara)
- 25+ Successful ASIC and FPGA Products
- 10+ Software Projects
- Team holds 68 patents
- Esencia holds 3 patents in EScala Design Platform

Core Business

- Design Services
  - Turn-key services from spec to Production
  - FPGA & Emulator platforms
- EScala Design Platform
  - Generates application specific configurable VLIW processor cores
- Software / Firmware / Driver Development
  - Windows, Linux & Android platform
- Soft IPs for Security and DSP Solutions

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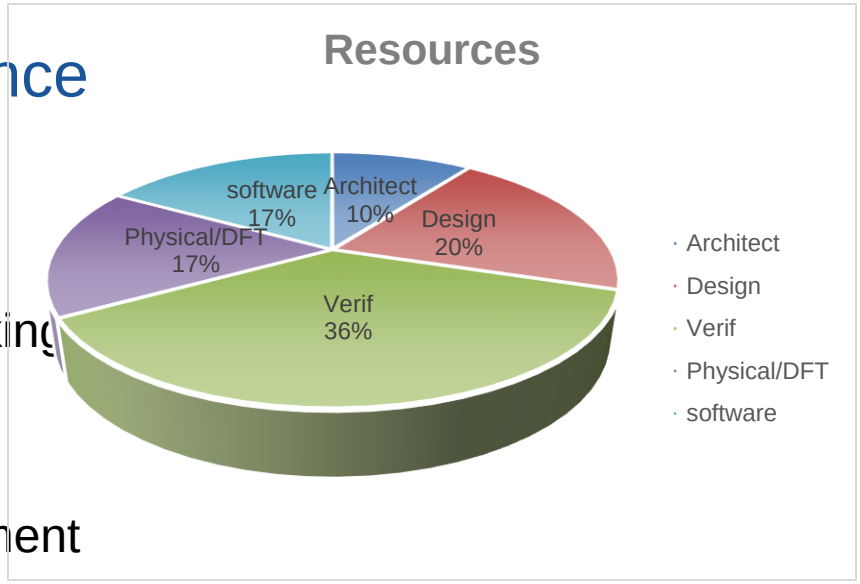
Expertise – Skills and Experience



Proven track-record

- Video/Image/Signal processing
- Wireless communication and Networking
- ASIC/SoC Architecture and Design
- FPGA Platforms
- Software / Firmware /Driver Development
- Deep Expertise in Low Power SoC design flow
- Physical design/Mixed Signal Design
- Product/Test Engineering

Team

- System Architects
- SOC/ASIC/FPGA architects
- Front-End SOC/ASIC/FPGA Design & Verification engineers
- Backend SOC/ASIC Design Engineers and Product Engineers
- Software, Firmware, Driver

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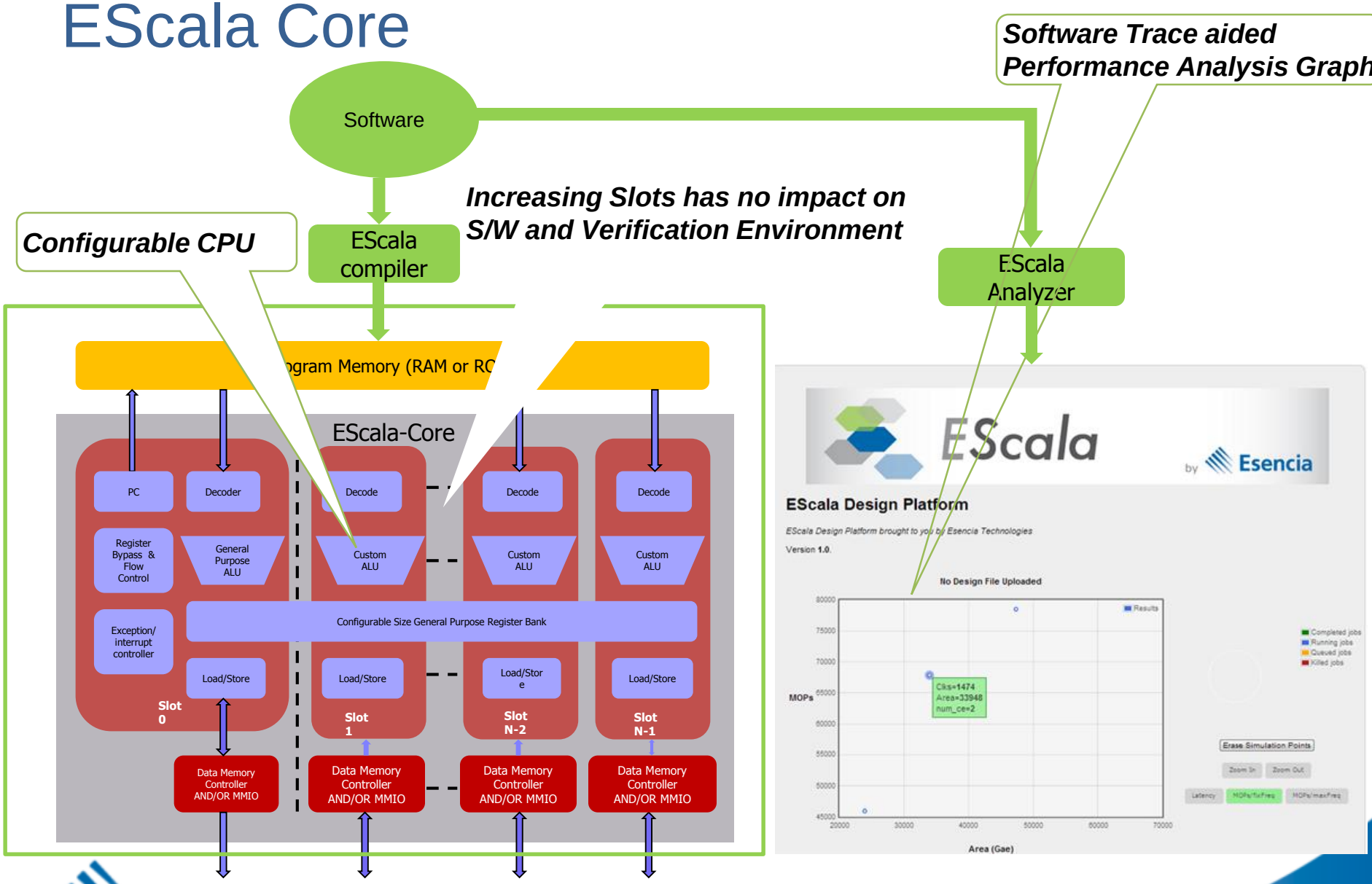
Escala: Configurable processor IP

- Configurable CPU
- Seamless scaling of CPU Horse Power
  - Adding ALU slots
  - Adding operand fetch paths (data memory instance)
- Software Trace Architecture Analysis
  - provides exact measurement of performance across different design points as controlled by design constraints
- EScala Software Development kit
  - Maps C/C++ algorithms (programs) to executable binaries
  - Used for design exploration while hardware design is flexible
  - Locked for specific chosen design -- allowing for multiple algorithms, enhancement, modifications, and corrections to be made after hardware design is frozen

EScala Core



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Other IP Cores:

- **Security Cores**
  - AES
  - DES/DES3
  - SHA-1/MD5
  - ARC4
- **Communication-Cores**
  - Configurable FFT core Generator
  - Viterbi Decoder
  - Reed Solomon Codec
  - Matlab/ RTL-DSP component library
- **Verification IPs for UVM**
  - MIPI
  - AHB/APB, AXI
  - SPI, I2C, JTAG
  - FIR, Correlators
- **ASIC Flow**
  - RTL generation flow
  - UVM Infrastructure
  - Auto DFT insertion flow
  - 40nm/28nm and 16nm Physical design flows.

Customer Success Stories