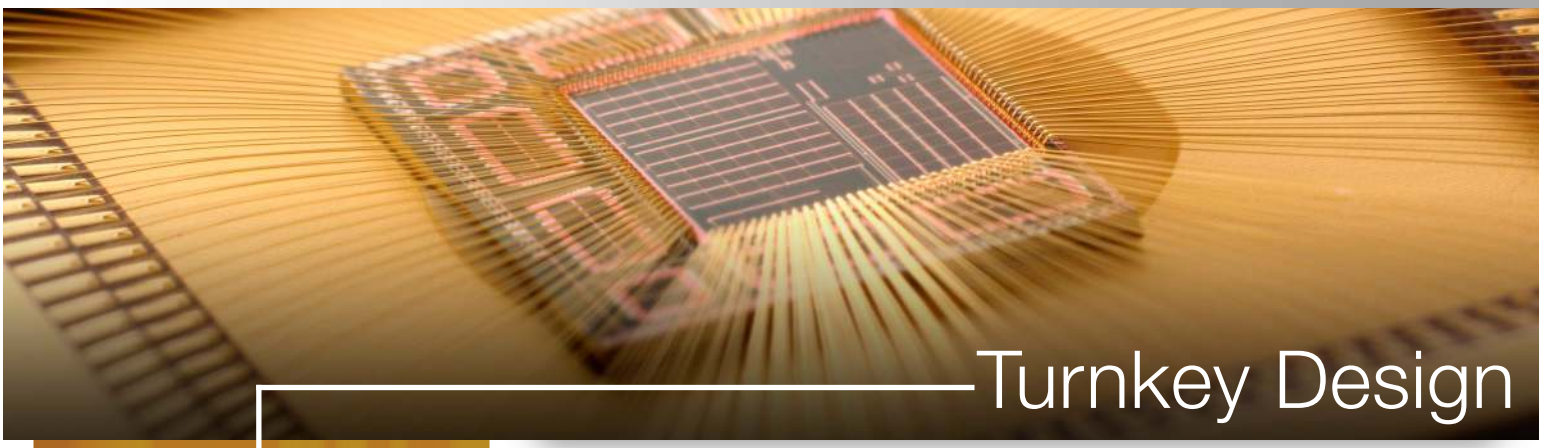
asicNorth

Bringing Analog / Mixed-Signal to Asic Design



Turnkey Design

asicNorth provides the ability to leverage new technology to make products smaller, faster and less expensive to produce.

Our team of multi-disciplined engineers can take a complex embedded system and transform it to a highly integrated single chip solution which can improve almost every aspect of the product.

asicNorth designers use best practices when migrating our customers design to a more productive incarnation. Quality and functional integrity are our first priority as we craft the next generation of their product.

For more information on asicNorth's Premier VLSI Design Services, please contact:

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Imagine the Benefits of an Integrated Solution

ENGAGEMENT PROCESS

The process of creating a custom ASIC for your application will follow a predictable sequence of events:

1. The first step is always for the engineering team to get a clear picture of the ASIC requirements. Technical & Physical specifications, expected environmental and electrical conditions are defined, required product lifetime is documented and cost constraints are identified.

2. A sizing is completed by asicNorth engineering which identifies solution options as well as estimates of all costs such as Non-Recurring Engineering (NRE) for the development, hardware, characterization, and ASIC qualification.

3. Next, we will collectively look at all aspects of the business case to see if it makes sense to move forward. There needs to be convincing evidence that the Return on Investment (ROI) will come in an acceptable frame of time (for both the customer and asicNorth).

4. If approved, Phase 1 begins. During this stage a final decision is made as to the technology which will be used and the new ASIC is designed and verified (through simulation). Multiple internal and customer design reviews are conducted to compare simulated device performance to specification, to discuss how the design effort is proceeding and to validate any assumptions made during the sizing stage. Once the final design review is completed, the customer approves moving to Phase 2, which is the fabrication and testing (Characterization) of the new ASIC.

5. Phase 2 entails the manufacture, packaging, and testing of the ASIC. The design database is submitted for fabrication and simultaneously, work is started to prepare for device testing. This involves making packaging arrangements and creating a test environment which allows all ASIC features to be verified. Once the ASIC silicon exits fabrication, asicNorth coordinates the packaging, initial test, and full characterization. A comprehensive Characterization report is published and reviewed with the customer.

6. Assuming the first pass hardware is production worthy, and is approved by the customer, production hardware is ordered and a plan is developed for Qualification and production ramp. JEDEC standards as well as customer requirements drive the level of qualification that is specified. A Manufacturing test plan is developed, documented and implemented, Typically, Qualification is run on parts from several lots of production hardware in an effort to determine estimates of product lifetime. Once qualification is successfully completed, the design is turned over to Supply Chain management which will subsequently coordinate all activities leading to fully tested components being shipped, as specified by the customer, to appropriate customers or contract manufacturers.

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Imagine the Benefits of an Integrated Solution *(continued)*

MIXED SIGNAL ASIC DESIGN METHODOLOGY

asicNorth creates VLSI components utilizing best of breed development processes. We recognize that such an endeavor represents a significant financial commitment by our customer and consequently believe that good communication is a top priority. As an example, let's assume the goal of developing a mixed signal (Analog & Digital) part as a replacement for an existing component. The design methodology applied would be very similar to the following:

1. A full specification of the device is required which fully details all aspects of the final component. This document can be an existing document, an update to the old one, or a completely new description. Although asicNorth can develop this document, the customer has responsibility of review and approval. This stage is very important because it becomes the primary reference point for the development effort that follows. Note that the specification must provide detailed performance requirements including nominal requirements as well as best/worst case values.

2. An architectural review is conducted where senior asicNorth engineers evaluate the specification and create a block diagram of the solution. Final Technology decisions are made at this stage as well as the development of a project plan which details the development schedule, major milestones (including major technical reviews), and engineering resource allocation. It is subsequent to this stage that the actual design stage for the ASIC commences.

3. The engineers at asicNorth subscribe to the belief that Integrated Circuits should be developed using a "Top-Down" design approach. This approach simply means that the entire design will be described behaviorally prior to the design of the underlying elements. Mixed Signal VLSI design involves the coordinated efforts of many engineering specialties. One of the responsibilities of the senior engineers is a detailed functional and structural description of every element in the block diagram. Although subject to change as the design effort progresses, these descriptions show the interactions between all design elements. It is with this information that the engineers who have responsibility for each specific block will create a behavioral representation of the block's operation. This behavioral will be written in Verilog, Verilog A,or Verilog AMS, whichever is the most appropriate. The engineer responsible for the top level design writes the interconnection of these blocks using structural Verilog. At this point, a Mixed Signal verification engineer is assigned to begin the process of writing simulation "test-cases" which will verify that the Verilog description accurately models the behavior of the Integrated Circuit described in the specification.

4. The engineering team is now in the Phase 2 of the design effort. Underlying design is proceeding where actual circuits are being developed and simulated at the schematic level. Simulations are run at process, temperature, and voltage corners (typically 12 to 15 cases) to verify the block performance under key process and environmental conditions. Depending on circuit functionality, Monte Carlo type of simulations are run to detect possible sensitivities to device mismatch. Digital circuits are synthesized to point to an appropriate digital library and timed to worst and best case conditions (insuring > 0ns slack for all Setup and Hold checks). As these circuits are completed, transistor level netlists (for Analog circuits) and logic block netlists (with estimated wiring) are included in the top level simulations to verify consistency between the actual design and the original behavioral representation. Phase 2 of the design effort will be completed when all underlying blocks are at this level. We are now ready for the first major design review with Senior asicNorth experts and Customer representatives.

5. Typically, action items are identified and tracked during the preliminary design review. The project manager has responsibility for tracking these items and insuring they are closed prior to the final (pre-manufacture) design review. Both the Analog and Digital engineering teams are now in Phase 3 of the design effort and involved in creating the physical realities of their designs in anticipation of final integration. For both teams, once the physical designs are created, simulations with extracted netlists are run. The extracted netlists include all parasitic resistances and capacitances associated with wiring and power distribution systems as well as element parasitics associated with device and well proximity for the analog circuits. At the top level of the design, the responsible engineer is responsible for verifying that the power distribution systems are accurately modeled for top level mixed mode simulations. As the design is heading toward final integration, Logical vs. Physical (LVS), Design Rule checks (DRC), and appropriate reliability checking are run an all elements as well as the fully integrated design. Once these efforts are completed, the team is prepared for the critical design review.

6. The final stage of the design effort (Phase 4) begins at the conclusion of the critical design review. A Compliance matrix has been created which identifies any discrepancies between design performance and the original specification. Senior asicNorth engineering, development project manager, and senior customer engineers evaluate the compliance matrix and decide which, if any, of the non-compliances can be waived. Based on these guidelines, the design effort is completed with all identified non-compliances resolved. The final design database is prepared for release to manufacture (RTM). A final meeting is held where customer representatives sign off on the release to the fabrication facility.

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