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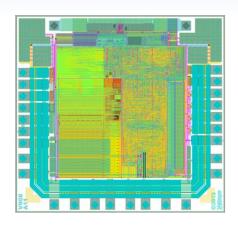
RADLogic

www.radlogic.com.au

Rob Clarke

Mixed-Signal IC Design Services

From Concept

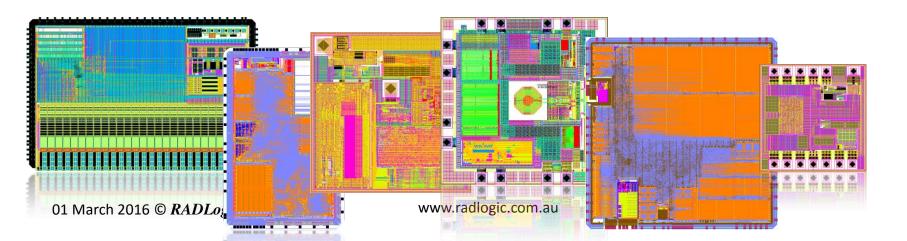


To Reality



CMOS Analog, Digital and Mixed-Signal IC Design Services

- Incorporated in 1990, currently 5 engineers, extensive experience.
- Full or Partial Design Services, offered world-wide.
- Not a manufacturer, but can assist customers with Wafer Foundry Interface, etc.
- Technology & Applications determined by our customers
- 10,000 to 10M transistor complexity
- Typical Processes: CMOS 130nm & 180nm, 55nm, 6-layer metal



```
module adc_format
(
  output [15:0] out, // Output to memory (for pads use out[15:4])
  input [21:0] in, // Inout from decimator (before any limiting)
  input [2:0] osr, // Oversampling Ratio
  input [3:0] shift, // Selector for 16 bits from the 21
  input use_unsigned // dont convert to 2's complement is asserted
);
  wire [20:0] jamout; // intermediate signal all 1's for limited

wire [20:0] decout; // Decimator output (before shifter)

wire osr128; // osr[]=000 128x oversampling
  wire osr64; // osr[]=010 32x oversampling
  wire osr32; // osr[]=010 32x oversampling
```

- Full Chip Design and Development
- Analog and Digital IP Development
- Test Development & Support
- HDL (VHDL, Verilog), Analog Design, Simulation, Layout and Verification
- ** RFID, RF, USB, Processor Architecture, Protocol Culture (International September 1997) (Conference of the International September 19
- Mentor, Cadence, Synopsys Design Tools







- Standard Protocols: ISO 14443, NFC, ISO 15693, ISO 18000-3 Modes 1,2, UHF EPC Gen2/ISO18000-6
- Characteristics:
 - RF Powered.
 - Low Power, Low Cost, Low Pin Count (2 pins), small chips.



- AFE includes Rectification, Voltage Regulation, Clock extraction/ generation, Command demodulation, Reply modulation.
- Digital includes Command Decoding, Protocol Engine, Memory Management, Security Features (e.g., SHA).
- Protocol Engine Generator: Rapidly creates low-power, minimal hardware that is extensible (interfaces to wired COMMs, security devices, etc).
- RADLogic licenses a synthesisable digital logic core for the EPC Gen2 UHF RFID Protocol, and also a UHF AFE design.

Example Applications





* RFID:

Authentication (Drugs, Security, Print Cartridges), Tracking (Medical, Aeronautical), Tagging (e.g, blood), Gaming (chips in chips),

Meter Reading, ...

USB: Hubs, Bridges & Peripherals

Medical: Neural Stimulation and Response measurement

Sensors: Temperature, Capacitive Touch, Optical, Frost, etc.

Controllers: Display Controllers & Microcontrollers

Silicon Fingerprints: Inherent process variation









Summary & Experience

₹/= RADLogic

Analog Experience:

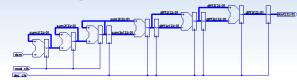
Power Supplies, PLL, DLL, Demodulators, modulators, Amplifiers, Filters & Comparators, ADC & DAC (Sigma-Delta, Switched Capacitor, Resistive), RF Transmission (900MHz), Memory Design (RAM, ROM, EEPROM/MTP), I/O Pads, ...

Digital Experience:

Processor Architecture, State Machine & General Logic design, HDL Coding, Test benches, High Level Modelling, FPGA prototyping, Logic Synthesis, Place & Route, Timing Closure, etc.

Other

- High Voltage Processes
- Printed Electronics (Silicon Ink)
- Optical sensors (Photo-sensors and SPADs)
- MEMS (Printer Ink Application)
- Liquid Crystal on Silicon (LCOS)







7

Thankyou for Listening



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Chip Design on your doorstep, anywhere.