

# R\_AFE\_UHF\_S180\_4M\_BB

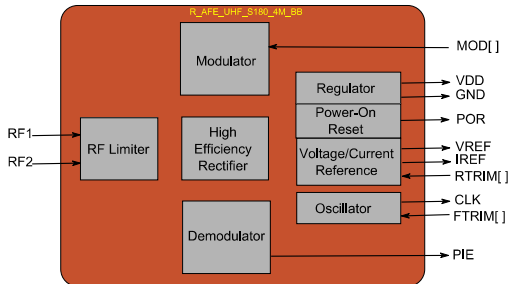
## Passive UHF RFID Analog Front End

### Overview

The **R\_AFE\_UHF\_S180\_4M\_BB** IP Block is a low power analog front end for passive UHF RFID systems compatible with EPCGlobal Class 1 Gen2 / ISO18000-6C standards.

### Features

- The Balanced RF front end (RF limiter with ESD protection): Limits the input levels during high RF fields and ESD events.
- Modulator: Programmable levels of impedance modulation for backscatter control.
- Rectifier: A high efficiency rectifier for low RF field operation. Adaptable to suit application needs.
- Power on reset (POR) circuit
- Voltage and Current Reference
- Trim-able  $\sim$ 2MHz Local Oscillator

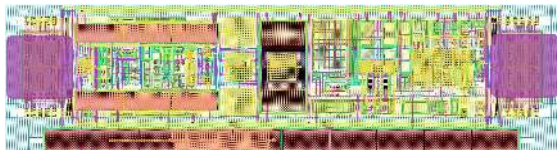


### Specifications

- Output supply voltage 0.8 to 1.8v. Supply regulation commences at  $\sim$ 1.65v.
- 0.55v voltage reference with a 22.5nA PTAT current sink.
- 2MHz local oscillator
- Power-on-reset: de-asserts at supply level  $\sim$ 825mV with a 40us onset delay and incorporating  $\sim$ 25mV hysteresis.
- Current consumption 1.5uA
- Input Impedance Parameters 15-j121 at 900MHz
- Maximum RF Field Strength +20dBm
- Size 0.063mm<sup>2</sup> (including RF pads)
- The RF front end is designed to be paired with RADLogic's EPC Gen2 digital core and suitable memory.

### Technologies

Currently designed for Silterra CL180G 0.18u 4LM CMOS process. The design is portable to other processes.



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