

IP BUILDING BLOCK DIAGRAM

The ADX300M10B40G is a Continuous Time (CT) $\Delta\Sigma$ Analog to Digital Converter (ADC) with built-in Anti-Aliasing Filters (AAF) and digital Decimation Filters.

It applies oversampling and captures the differential analog input signal with a 5 GSPS sampling clock, at the easy to drive continuous time analog input.

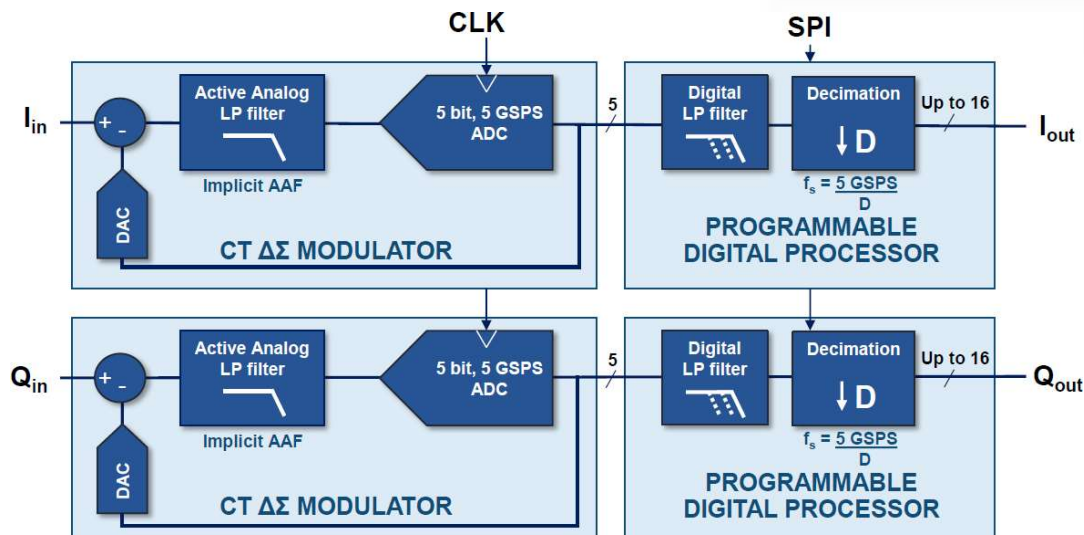
The CT $\Delta\Sigma$ Modulator loop includes inherent Anti-Aliasing Filter. This significantly reduces analog filter requirements compared to Nyquist ADCs. A robust multi-bit CT $\Delta\Sigma$ architecture ensures low sensitivity to clock jitter.

The ADX300M10B40G contains programmable digital decimation filters. These can be used to reduce data-rate and ensure compliance with the system requirements. The possible access to very high sample-rates, guarantees for excellent timing accuracy.

FEATURES

- 5 GSPS Internal Sampling Rate
 - Integrated Decimation Filter adjusts Output Sampling Rate
- 300 MHz Full Performance Bandwidth
- 10-bit Resolution
- 2.0Vpp Full Scale Range
 - Resistive input impedance
- Performance @ $f_{in}=10\text{MHz}$:
 - SNR= 49dBFS
 - SNDR = 48dBFS
 - THD = 62dBc @ $A_{in} = -1\text{dBFS}$
 - SFDR = 62dBc @ $A_{in} = -1\text{dBFS}$
 - ENOB = 7.5bit
 - Channel Isolation > 75dB
- 1.8V analog and 1.0V digital supplies
- Full Power consumption: <175mW/Ch
 - Stand-By and Power-Down Modes
- 40nm TSMC CRN40G process
 - 7 metals used
 - TGO and LVT options used
- Compact Die Core Area
 - <1.5 mm²

IP BUILDING BLOCK DIAGRAM



STATUS

Pre-Silicon

SCALINX SMART CONVERSION BUILDING BLOCKS

- **ADX:** Dual Channel CT $\Delta\Sigma$ I/Q ADCs
 - 5 GSPS, 62.5MHz, 14-bit
 - 5 GSPS, 125MHz, 12-bit
 - 5 GSPS, 200MHz, 12-bit
 - 5 GSPS, 300MHz, 10-bit
 - All ADX IPs are also available as single and quad channel building blocks
- **CLX:** Clock Synthesizer
 - 5GHz output clock rate
- **AGX:** Programmable Gain Amplifier
 - 14-40dB gain range
 - 1000MHz BW
- **DAX:** 16-bit Auxiliary DAC
 - ± 300 mV DC voltage adjustment
- **IOX:** Complete LVDS Transmitter
 - Digital protocol and Analog Physical Layer
 - Up to 1250Mbps

Along with described building blocks, Scalinx can provide solutions including wide-band DACs.

SCALINX SMART CONVERSION PLATFORM

The ADX300M10B40G IP building block is integral part of the Scalinx *Smart Conversion Platform*.

The use of the *Smart Conversion Platform* reduces system development cost for data converter projects with analog bandwidths between 5 MHz and 600MHz.

The *Smart Conversion Platform* uses wideband CT $\Delta\Sigma$ ADC technology. This enables solutions where bandwidth vs. resolution trade-off as well as signal filters are implemented in programmable digital circuitry.

The flexibility and programmability ingredients of the *Smart Conversion Platform* combined with appropriate IP functional blocks furnish fast and flexible path to single hardware solution for various specifications

These features make the *Smart Conversion Platform* an ideal starting-point for digitizer ASIC projects demanding high analog bandwidths.

SMART CONVERSION PLATFORM BLOCK DIAGRAM

