IP Building Block

ADXSCIP1-40G

Dual Channel Programmable CT ΔΣ I/Q ADC:5GSPS

IP BUILDING BLOCK DIAGRAM

The ADXSCIP1-40G is a Continuous Time (CT) ΔΣ Analog to Digital Converter (ADC) with built-in Anti-Aliasing Filters (AAF) and digital Decimation Filters.

It applies oversampling and captures the differential analog input signal with a 5 GSPS sampling clock, at the easy to drive continuous time analog input.

The Programmable CT ΔΣ Modulator loop includes inherent Anti-Aliasing Filter. This significantly reduces analog filter requirements compared to Nyquist ADCs. The Modulator can be programmed from 20MHz Bandwidth and 16-bit resolution to 300 MHz Bandwidth at 10-bit resolution. A robust multi-bit CT ΔΣ architecture ensures low sensitivity to clock jitter.

The ADXSCIP1-40G contains programmable digital decimation filters. These can be used to reduce data- rate and ensure compliance with the system requirements. The possible access to very high sample- rates, guarantees for excellent timing accuracy.

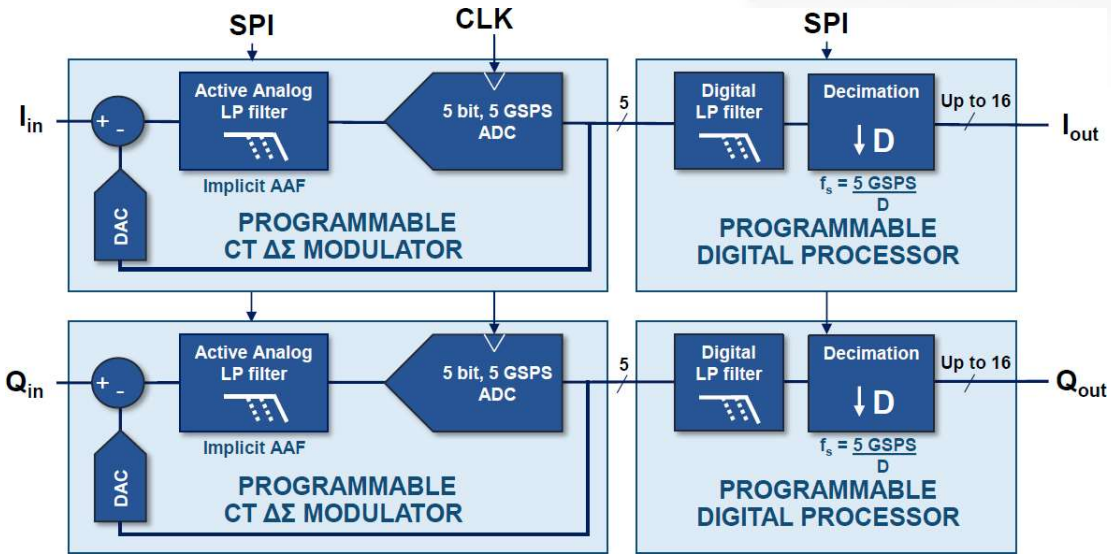
FEATURES

- 5 GSPS Internal Sampling Rate
  - Integrated Decimation Filter adjusts Output Sampling Rate
- 20-300 MHz Full Performance Bandwidths
- 2.0Vpp Full Scale Range
  - Resistive input impedance
- 5 Bandwidth modes:
  - 20MHz, 16-bit resolution
  - 62.5MHz, 14-bit resolution
  - 125MHz, 12-bit resolution
  - 200 MHz, 12-bit resolution
  - 300 MHz, 10-bit resolution
- Performance @ Fin=10MHz:
  - SNR: 49 - 75dBFS @10 – 16-bit
  - SNDR = 48 – 74 dBFS @ 10 - 16-bit
  - THD = 62-78 dBc@ 10 – 16-bit
  - SFDR = 62-80 dBc@ 10 – 16-bit
  - ENOB = 7.5-12bit@ 10 - 16-bit
  - Channel Isolation > 75dB
- 1.8V analog and 1.0V digital supplies
- Full Power consumption: <175mW/Ch
  - Stand-By and Power-Down Modes
- 40nm TSMC CRN40G process
  - 7 metals used
  - TGO and LVT options used
- Compact Die Core Area
  - <1.5 mm2

STATUS

Pre-Silicon

IP BUILDING BLOCK DIAGRAM



SCALINX SMART CONVERSION BUILDING BLOCKS

- **ADX**: Dual Channel CT ΔΣ I/Q ADCs
  - 5 GSPS, 62.5MHz, 14-bit
  - 5 GSPS, 125MHz, 12-bit
  - 5 GSPS, 200MHz, 12-bit
  - 5 GSPS, 300MHz, 10-bit
  - All ADX IPs are also available as single and quad channel building blocks
- **CLX**: Clock Synthesizer
  - 5GHz output clock rate
- **AGX**: Programmable Gain Amplifier
  - 14-40dB gain range
  - 1000MHz BW
- **DAX**: 16-bit Auxiliary DAC
  - ±300 mV DC voltage adjustment
- **IOX**: Complete LVDS Transmitter
  - Digital protocol and Analog Physical Layer
  - Up to 1250Mbps

Along with described building blocks, Scalinx can provide solutions including wide-band DACs.

SCALINX SMART CONVERSION PLATFORM

The ADXSCIP1-40G IP building block is integral part of the Scalinx ***Smart Conversion Platform***.

The use of the ***Smart Conversion Platform*** reduces system development cost for data converter projects with analog bandwidths between 5 MHz and 600MHz.

The ***Smart Conversion Platform*** uses wideband CT ΔΣ ADC technology. This enables solutions where bandwidth vs. resolution trade-off as well as signal filters are implemented in programmable digital circuitry.

The flexibility and programmability ingredients of the ***Smart Conversion Platform*** combined with appropriate IP functional blocks furnish fast and flexile path to single hardware solution for various specifications

These features make the ***Smart Conversion Platform*** an ideal starting-point for digitizer ASIC projects demanding high analog bandwidths.

SMART CONVERSION PLATFORM BLOCK DIAGRAM