SCALINX
NEW ART OF SIGNAL CONVERSION

IP Building Block

CLX5000M40G

Clock Synthesizer 5000MHz

IP BUILDING BLOCK DIAGRAM

The CLX5000M40G is a dual programmable gain amplifier with 14-40dB gain range, and a flat passband from DC to 300MHz

It has embedded ground isolation, with a ± 1.8V input supply, and output supply from 1.8V to GND.

With a high input impedance, the CLX5000M40G is easy to drive, and it is an excellent choice for wide band ADC driver in applications where signal gain is required.

The low input referred noise ensures excellent Signal to Noise ratio

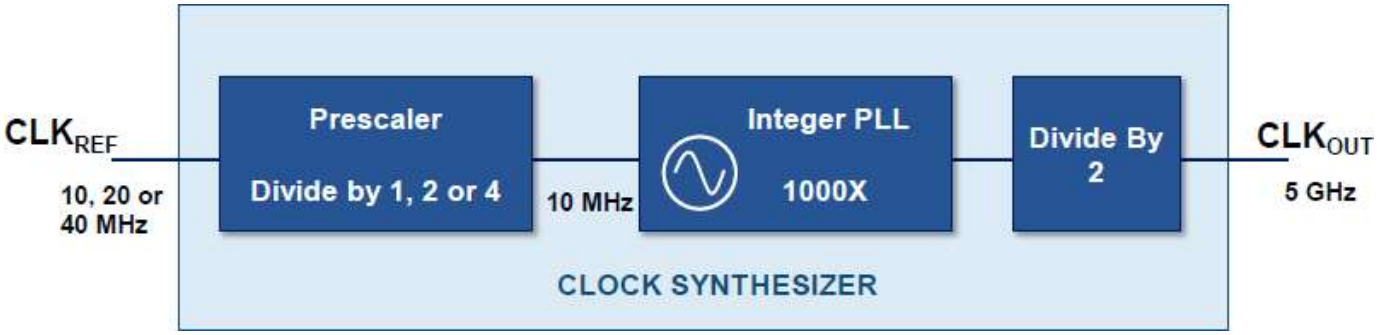
FEATURES

- 10, 20 and 40 MHz reference clocks
  - ±1% Input frequency accuracy
  - 40-60% Duty cycle
  - 0.4 – 2 Vpp input level
- 5 GHz output frequency
  - <1psrms aperture jitter
- <1ms locking time
- 1.8V supply voltage
- Full Power consumption: <20mW
  - Stand-By and Power-Down Modes
- 40nm TSMC CRN40G process
  - 7 metals used
  - TGO and LVT options used
- Compact Die Core Area
  - <1 mm^2

STATUS

Pre-Silicon

IP BUILDING BLOCK DIAGRAM



SCALINX SMART CONVERSION BUILDING BLOCKS

- **ADX**: Dual Channel CT ΔΣ I/Q ADCs
  - 5 GSPS, 62.5MHz, 14-bit
  - 5 GSPS, 125MHz, 12-bit
  - 5 GSPS, 200MHz, 12-bit
  - 5 GSPS, 300MHz, 10-bit
  - All ADX IPs are also available as single and quad channel building blocks
- **CLX**: Clock Synthesizer
  - 5GHz output clock rate
- **AGX**: Programmable Gain Amplifier
  - 14-40dB gain range
  - 1000MHz BW
- **DAX**: 16-bit Auxiliary DAC
  - ±300 mV DC voltage adjustment
- **IOX**: Complete LVDS Transmitter
  - Digital protocol and Analog Physical Layer
  - Up to 1250Mbps

Along with described building blocks, Scalinx can provide solutions including wide-band DACs.

SCALINX SMART CONVERSION PLATFORM

The CLX5000M40G IP building block is integral part of the Scalinx ***Smart Conversion Platform***.

The use of the ***Smart Conversion Platform*** reduces system development cost for data converter projects with analog bandwidths between 5 MHz and 600MHz.

The ***Smart Conversion Platform*** uses wideband CT ΔΣ ADC technology. This enables solutions where bandwidth vs. resolution trade-off as well as signal filters are implemented in programmable digital circuitry.

The flexibility and programmability ingredients of the ***Smart Conversion Platform*** combined with appropriate IP functional blocks furnish fast and flexile path to single hardware solution for various specifications

These features make the ***Smart Conversion Platform*** an ideal starting-point for digitizer ASIC projects demanding high analog bandwidths.

SMART CONVERSION PLATFORM BLOCK DIAGRAM