IP Building Block

DAX16B40G

1-bit Auxiliary DAC: 16-bit resolution

IP BUILDING BLOCK DIAGRAM

The DAX16B40G is 1-bit ΔΣ Modulator DAC with 16-bit output resolution.

The use of a balanced ±1.8V analog supply voltage, allows output voltage covering ±300mV referred to Ground.

An Analog Low Pass Filter at the output ensures very high accuracy and low noise for the analog output voltage. The robust architecture also ensures very low output ripple voltage

The high frequency reference clock makes the DAX16B40G an ideal Auxiliary DAC for the Scalinx ADX ADC building blocks.

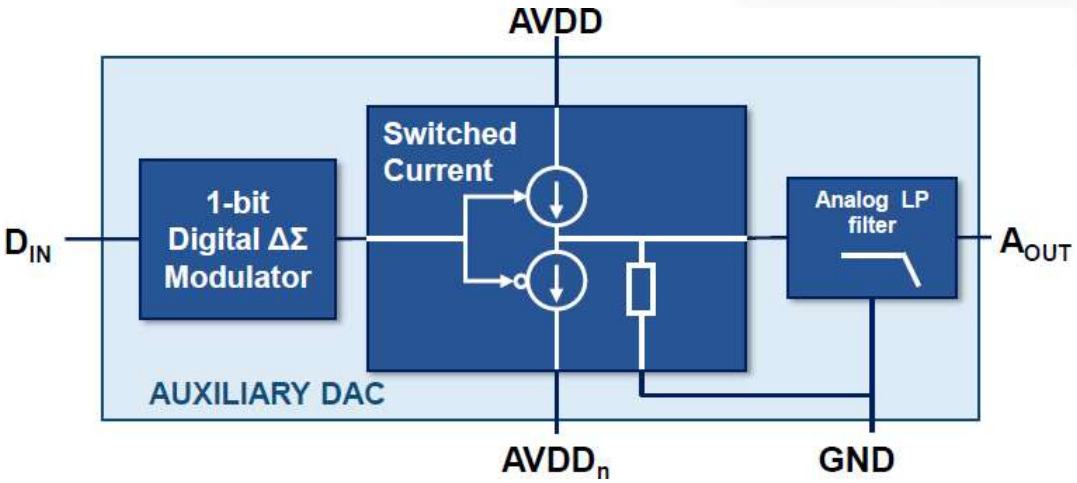
FEATURES

- 2.5 GSPS Internal Sampling Rate
  - 1-bit Digital ΔΣ Modulator
- 16-bit Resolution
- 4 KHz operation bandwidth
- ±300 mV Analog output range
- INL: ±7LSB
- Output ripple: 4 µVp-p
- Output Thermal noise: 10µVrms
- ±1.8V analog and 1.0V digital supplies
- Full Power consumption: <6mW
  - Stand-By and Power-Down Modes
- 40nm TSMC CRN40G process
  - 7 metals used
  - TGO and LVT options used
- Compact Die Core Area

STATUS

Pre-Silicon

IP BUILDING BLOCK DIAGRAM



SCALINX SMART CONVERSION BUILDING BLOCKS

- **ADX**: Dual Channel CT ΔΣ I/Q ADCs
  - 5 GSPS, 62.5MHz, 14-bit
  - 5 GSPS, 125MHz, 12-bit
  - 5 GSPS, 200MHz, 12-bit
  - 5 GSPS, 300MHz, 10-bit
  - All ADX IPs are also available as single and quad channel building blocks
- **CLX**: Clock Synthesizer
  - 5GHz output clock rate
- **AGX**: Programmable Gain Amplifier
  - 14-40dB gain range
  - 1000MHz BW
- **DAX**: 16-bit Auxiliary DAC
  - ±300 mV DC voltage adjustment
- **IOX**: Complete LVDS Transmitter
  - Digital protocol and Analog Physical Layer
  - Up to 1250Mbps

Along with described building blocks, Scalinx can provide solutions including wide-band DACs.

SCALINX SMART CONVERSION PLATFORM

The DAX16B40G IP building block is integral part of the Scalinx ***Smart Conversion Platform***.

The use of the ***Smart Conversion Platform*** reduces system development cost for data converter projects with analog bandwidths between 5 MHz and 600MHz.

The ***Smart Conversion Platform*** uses wideband CT ΔΣ ADC technology. This enables solutions where bandwidth vs. resolution trade-off as well as signal filters are implemented in programmable digital circuitry.

The flexibility and programmability ingredients of the ***Smart Conversion Platform*** combined with appropriate IP functional blocks furnish fast and flexile path to single hardware solution for various specifications

These features make the ***Smart Conversion Platform*** an ideal starting-point for digitizer ASIC projects demanding high analog bandwidths.

SMART CONVERSION PLATFORM BLOCK DIAGRAM