IP Building Block

IOX1250MTX40G

Complete LVDS Transmitter, up to 1.25Gbs

IP BUILDING BLOCK DIAGRAM

The IOX1250MTX40G a complete LVDS transmitter. It includes an analog physical level driver as well as a digital interface covering a set of operational modes. Both serialization modes and parallelization modes are supported. The outputs are organized in 10-bit or 20- bit wide transmit banks

A wide set of speeds is available through an internal clock divider in the Digital Interface.

The Digital Interface can be scaled to support from 1 to 4 input channels

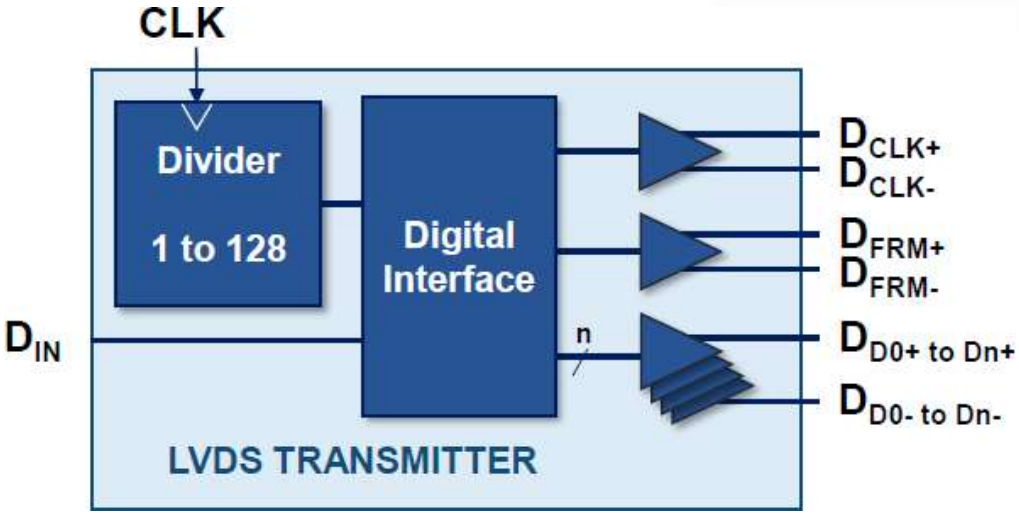
FEATURES

- Complete LVDS transmitter
  - Analog driver
  - Digital protocol
  - Parallelization Modes
  - Serialization modes
- Up to 1.25Gbps bit-rate
  - 1.5mA (RSDS) to 5.0mA driving strengths (3.5mA default)
- Internal termination option available
- 0.9V to 1.2V (default) common mode voltages
- 10-bit and 20-bit output banks
- 1.8V analog and 1.0 digital supply voltages
- Power consumption: 7mW/Ch
  - Stand-By and Power-Down Modes
- 40nm TSMC CRN40G process
  - 7 metals used
  - TGO and LVT options used

STATUS

Pre-Silicon

IP BUILDING BLOCK DIAGRAM



SCALINX SMART CONVERSION BUILDING BLOCKS

- **ADX**: Dual Channel CT ΔΣ I/Q ADCs
  - 5 GSPS, 62.5MHz, 14-bit
  - 5 GSPS, 125MHz, 12-bit
  - 5 GSPS, 200MHz, 12-bit
  - 5 GSPS, 300MHz, 10-bit
  - All ADX IPs are also available as single and quad channel building blocks
- **CLX**: Clock Synthesizer
  - 5GHz output clock rate
- **AGX**: Programmable Gain Amplifier
  - 14-40dB gain range
  - 1000MHz BW
- **DAX**: 16-bit Auxiliary DAC
  - ±300 mV DC voltage adjustment
- **IOX**: Complete LVDS Transmitter
  - Digital protocol and Analog Physical Layer
  - Up to 1250Mbps

Along with described building blocks, Scalinx can provide solutions including wide-band DACs.

SCALINX SMART CONVERSION PLATFORM

The IOX1250MTX40G IP building block is integral part of the Scalinx ***Smart Conversion Platform***.

The use of the ***Smart Conversion Platform*** reduces system development cost for data converter projects with analog bandwidths between 5 MHz and 600 MHz.

The ***Smart Conversion Platform*** uses wideband CT ΔΣ ADC technology. This enables solutions where bandwidth vs. resolution trade-off as well as signal filters are implemented in programmable digital circuitry.

The flexibility and programmability ingredients of the ***Smart Conversion Platform*** combined with appropriate IP functional blocks furnish fast and flexile path to single hardware solution for various specifications

These features make the ***Smart Conversion Platform*** an ideal starting-point for digitizer ASIC projects demanding high analog bandwidths.

SMART CONVERSION PLATFORM BLOCK DIAGRAM