mirafra
TECHNOLOGIES

Mirafra Design Services
Case Studies

Confidential – Do not share

Multi-core ARM-based CPU Subsystem and SoC Verification

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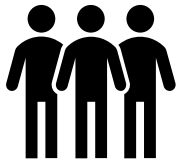
- Owned functional verification of M7 and C55 ARM Cores CPU Sub-system, IP, Peripherals of SOC
- Verification of ARM core sub-system using C, assembly, System Verilog and UVM methodology
- Integration of Bus, IPs, VIPs for functional verification of SOC
- Verification of primary external interfaces: DDR4/DDR5, PCIe
- Verification of general external interfaces: JTAG, I3C, SPI, UART, GPIO,SDRAM
- Verification of interrupts by creating them functionally from all IPs and verifying that both M7 and A55 ARM processors were clearing them through ISR
- Formal verification for connectivity
- Enabling X-prop for all subsystems and SOC
- Gate level simulations (zero delay, min and max corners)
- Power aware verification
- Sign-off through functional coverage, regression pass rate
- Code coverage for in-house developed IPs



1 DV Lead
14 engineers

1 year

ODC with ownership of deliverables

Verification of CXL-Based Smart Network Controller for Memory SOC

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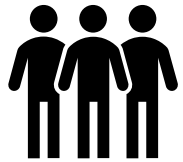
- SOC level :
  - Verification of primary external interfaces: DDR4/DDR5, PCIe, CXL
  - Verification of external interfaces: JTAG, I3C, QSPI, UART, GPIO
  - Formal verification for connectivity
  - Gate level simulations (zero delay, min and max corners) and Xprop
  - Power aware verification
  - SOC feature detailed test plan and test plan for each subsystem
  - UVM Based constrained random verification environment
  - Sign-off through functional coverage, regression pass rate
- Subsystem :
  - PCIe (32 lanes), CXL Controller Block, Performance Resource Director, System Level Cache, DDR Memory Block, Security Block
  - SOC with stub based subsystem verification



2 DV leads
16 engineers

12 months

ODC with ownership of deliverables

Provides the ability to expand or pool DDR memory, PCIe/CXL storage/memory
Connect to numerous host servers with high-bandwidth and low-latency
High speed peripherals like USB, NAND

DFT - ATPG to Post Silicon for Graphics Chip

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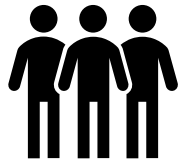
- Complete ownership of DFT/ATPG for 3 variants of a large graphics chip
  - DFT for ~70 partitions
  - Stuck-At and At-speed pattern generation and simulation
  - Interface with RTL, PnR and ATE teams
  - Support power-on and silicon bring-up
- Flow enhancement for efficiency

Tessent, Test Kompress, ITPP, Tcl



1 lead
10 engineers

2.5 years - ongoing

OCB at client site with ownership of deliverables

Physical Design : PNR & Timing Closure of Multiple Partitions

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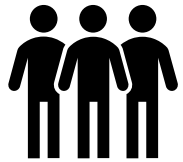
- Netlist handoff & constraints validation
- Floorplan Closure with interface from RTL & Synthesis teams
- Understanding of UPF and design in multiple Low Power Design Scenarios
- Clock Tree Synthesis, Skew balancing and Timing Closure
- Completed blocks by closing PV for all blocks

DC, Innovus, ICC2, Primetime
14nm, 10nm, 7nm, 1.1 GHz, 1.35 GHz, 2.2 GHz



2 leads
20+ engineers

2 years - ongoing

OCB at client site with ownership of deliverables

Emulation Of Fibre Channel Chip

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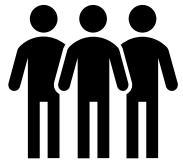
Prototyping/Emulation :

- The ASIC consisting of around 6 million ASIC gates is emulated in largest available Xilinx V7- 2000T FPGA.
- The board from Hitech Global "HTG-V7-PCIE-2000" has an additional SFP+ daughter card to communicate with Ethernet
- Convert ASIC design to FPGA compatible.
- Reset scheme for the emulation design.
- Clock scheme/ratio for the emulation design.
- Create memory wrappers and FIFOs for the emulation design.
- Implement the design using latest Xilinx Vivado Tool.
- Bit-stream Generation with no Timing Violation.
- Debug



1 Project Manager + 5 FPGA engineers

6 months

TNM

Synplify, Vivado, Verilog, C, Perl

FPGA Prototyping Of AI Vision Platform

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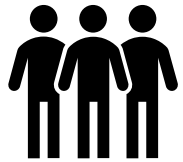
Deliver working FPGA Prototype of Complete SoC:

- Identify and select FPGA platform vendor
- Define deliverable for customer, software team and board design team
- Porting of ASIC IP for selected FPGA family, design partitioning, design verification.
- Synthesis, Place and Route, Timing Closure
- FPGA Bitstream and platform bring-up
- Linux OS and Application software bring-up for pre-silicon validation

Synplify, Vivado, Verilog, C, Perl



1 Project Manager + 1 Lead + 7 FPGA engineers

12 months

TNM

Post Silicon Validation – PnP Validation of Graphics Subsystem

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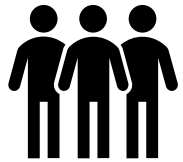
- Validate the Power and Performance of Test Vectors
- Execution and Debug on Multiple Platforms for Multiple generations
- Hands On Execution and Debug of Test Vectors
- Validation on bare metal and OS environments
- Automation
- Emulation workload launches, data post processing & publishing during pre-silicon phase and initial stepping

C, Python, Trace32, Bus analyzers, proprietary tools



1 lead
11 engineers

4 years - ongoing

OCB with ownership of deliverables