

SignOff
semiconductors

ABOUT US

Quality, Customer success & TTM are our key goals

8th
YEAR OF OPERATIONS

PD, RTL, CUSTOM LAYOUT, CKT DESIGN, VERIF, STA, METHODOLOGY

240+
ENGINEERS

Self driven, Motivated, Trained, Proactive, SignOff Family

200+
TAPE OUTS

Graphics, IoT, Automobile, N/W ICs, CPU, Modem, custom-ASIC, SoCs

Employee
Centric approach

Best Place to Work, Collective growth, learning, RnD, Sustainable model

ANVAY
IN HOUSE ASIC/SoC FLOW

Simple, Robust, Optimized, Dashboard, Automation

KAVERI
RISCV BASED ASIC

Robust, Low power, Customizable, Scalable

VISION

“Our vision is to be a leading semiconductor service company. Quality, Customer success & TTM are our key goals”

Motivation to start SignOff Semiconductors

“Lack of quality engineers, guidance & training in SemiCon industry motivated founders to quit their stable jobs at Intel and start SignOff Semiconductors”

How different we are?

“We never compromise on technical growth, developing right attitude & approach among engineers, strong work ethics, respect, care, concern and collective growth”



To build a strong talent pool



Respect, Care, Concern



Commitment & Work as a team



Grow & help others to grow



Strong work ethics



Quality & Sense of Urgency

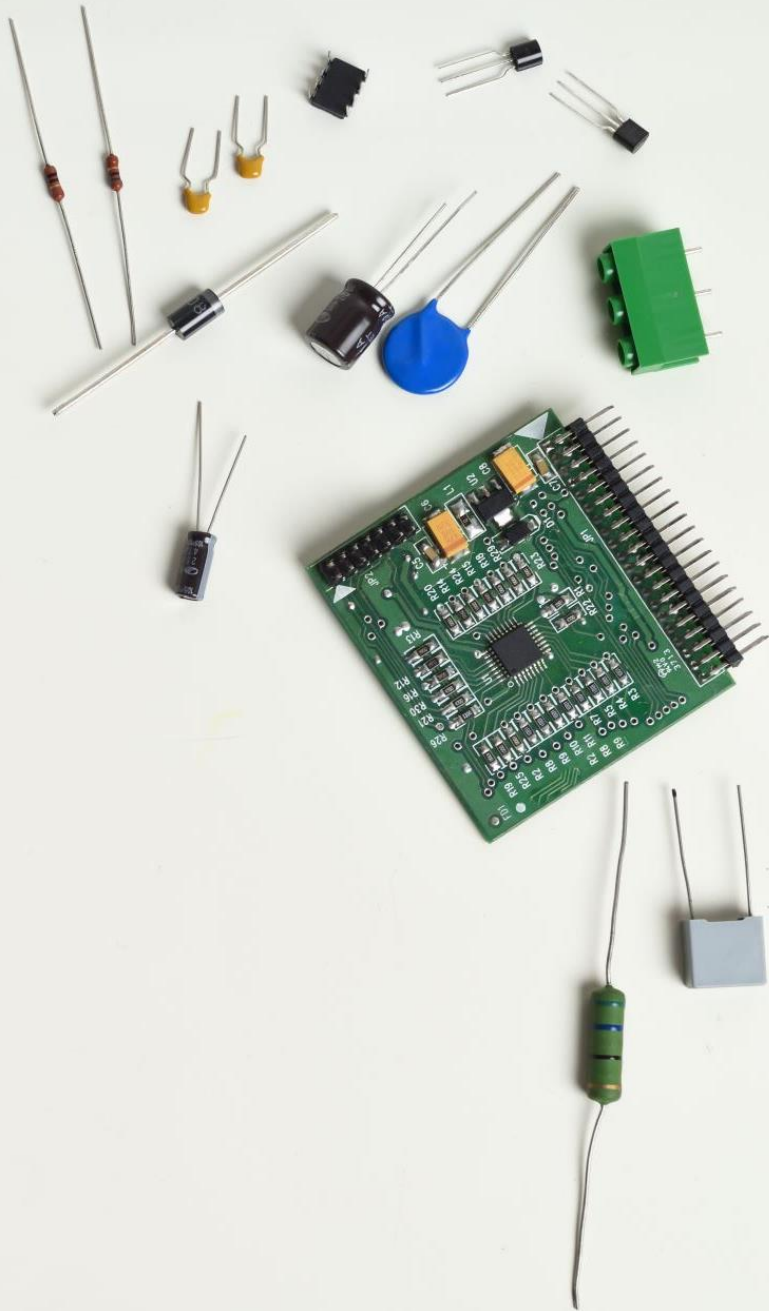
Powering IoT through Customized ASIC's

SignOff designing robust, reliable and scalable IoT based ASIC's

According to various reports, there would be more than 50 billion connected devices by the year 2020. From smart homes to smart cars and smart wearables & gadgets, the IoT market is impacting the way we do business along with changing the way we build things and experience them.

SignOff's capabilities in ASIC's for IoT:

- IoT Systems
- Product Differentiation through Customized ASICs for Sensor Hubs
- Turnkey IoT ASIC solutions



SERVICES

Quality & TTM are never compromised

DIGITAL & PHYSICAL DESIGN

- RTL Design.
- FPGA Design.
- Synthesis & STA
- Block level implementation with Low power expertise
- Full-Chip timing & Full-Chip floorplaning
- Physical Verification & EMIR
- Flow/methodology development.
- Custom ASIC development.

VERIFICATION

- Understanding spec & creating the test plan
- Creating verification environment using industry standard methodologies (SV, UVM, OVM)
- AMBA (AXI*, AHB*), RISC-V, SOC/IP, I2C, UART, Mem, VIPs.
- Gate level simulations. Verification closure through corner case verification, coverage closure and regression closure

CKT DESIGN & CUSTOM LAYOUT

- Analog/AMS Design & Layout
- Memory design & layout
- Library dev (schematic design, layout, characterization) & Benchmarking
- RF Design & Layout
- Analog Full Chip Closure
- LNA, PLL, DCO, TXPA, OPAMPs, PADDING, BGR, ADC, DAC, LDO

VERTICALS : AUTOMOTIVE, CLIENT & COMPUTING, MEM & STORAGE, SERVER & NETWORKS, COMMUNICATION (MODEMS), IOT

TECH Nodes: Intel:32, 14, 10 / TSMC:350, 180, 65, 90, 45/45GS(40), 28LP/HPC, 16FF/FFC, 7, 5 / GF:28, 14LPE, 22FDX / ST-Micro:28 FDSOI

Kaveri : Low Cost, Low Power Embedded Compute Solution

➤ Overview:

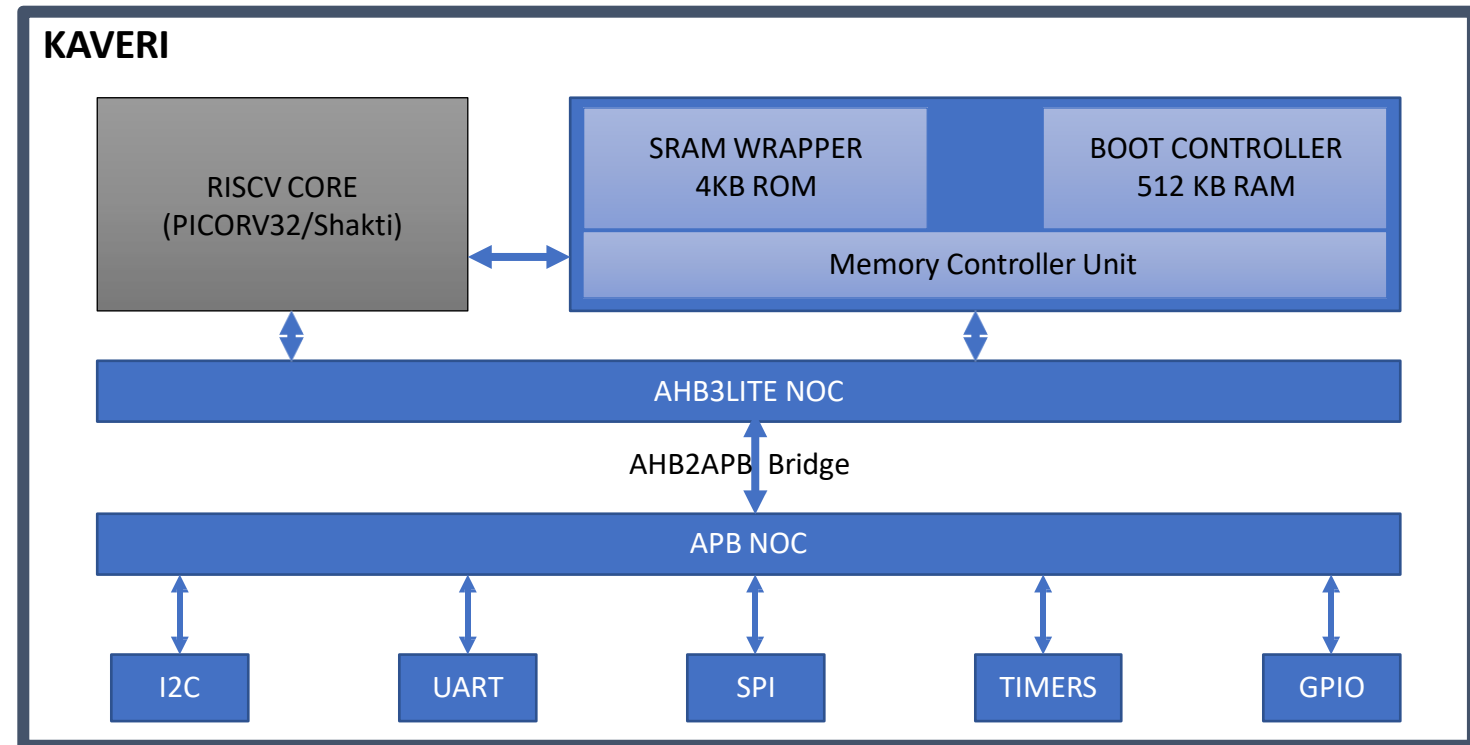
- ✓ PICORV32 based general purpose microcontroller solution.
- ✓ Low Cost, Low power compute.

➤ Highlights:

- ✓ Fully Verified. FPGA-Tested.
- ✓ Inhouse developed NOC and Peripherals.
- ✓ Multiple Firmware tested on FPGA (Display, Oximeter, Breadth Analyzer)

➤ Package

- ✓ ASIC Verilog, SDC
- ✓ Verification test suite.
- ✓ Scripts (ASIC Synth, PnR)



➤ Further Roadmap:

- ✓ Kaveri Silicon Solution (Ready for tapeout)
- ✓ RISC-V Core as Shakti (Under Development)
- ✓ NB-IOT enabled ASIC (Under definition)

Clients



Partnerships

EDA



FAB



IP



THE TEAM (Leadership)

We work together



GAURAV BANSAL

Co-Founder, Director



SOMASHEKHAR AMBALI

Co-Founder, Director



VIKRAM KHEMCHANDANI

Co-Founder, CEO



UTTAM SINGHAL

EVP – Signoff
MD – Signoff Canada



NARAHARI TR

Sr VP - Engineering



Manoj Subramanian

VP – HR & Operations



MANJUNATH V

Sr Director - Engineering



NITIN GUPTA

Director – AMS Layout



Praveen Mullasery

Director – Engineering







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