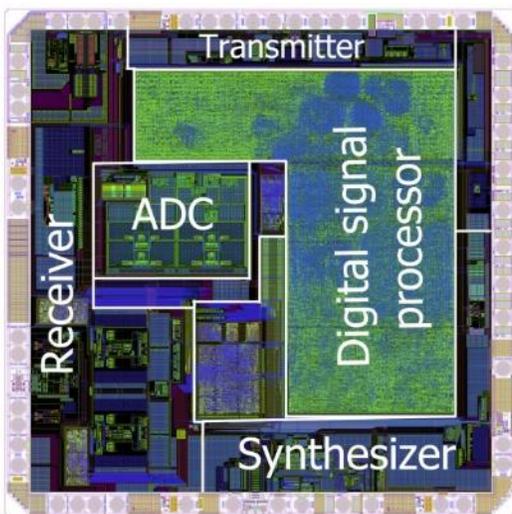


Company expertise

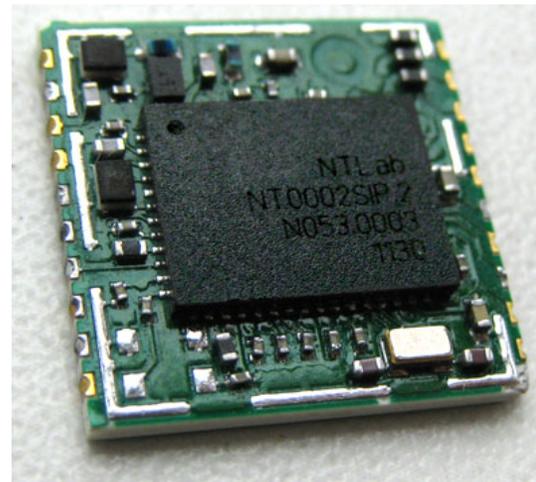
Business profile

NTLab is a vertically integrated center for electronics: from ICs to devices.
Design and production

Semiconductor IP & chips



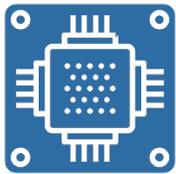
Integrated modules



Devices



NTLab services



ASIC & IP design

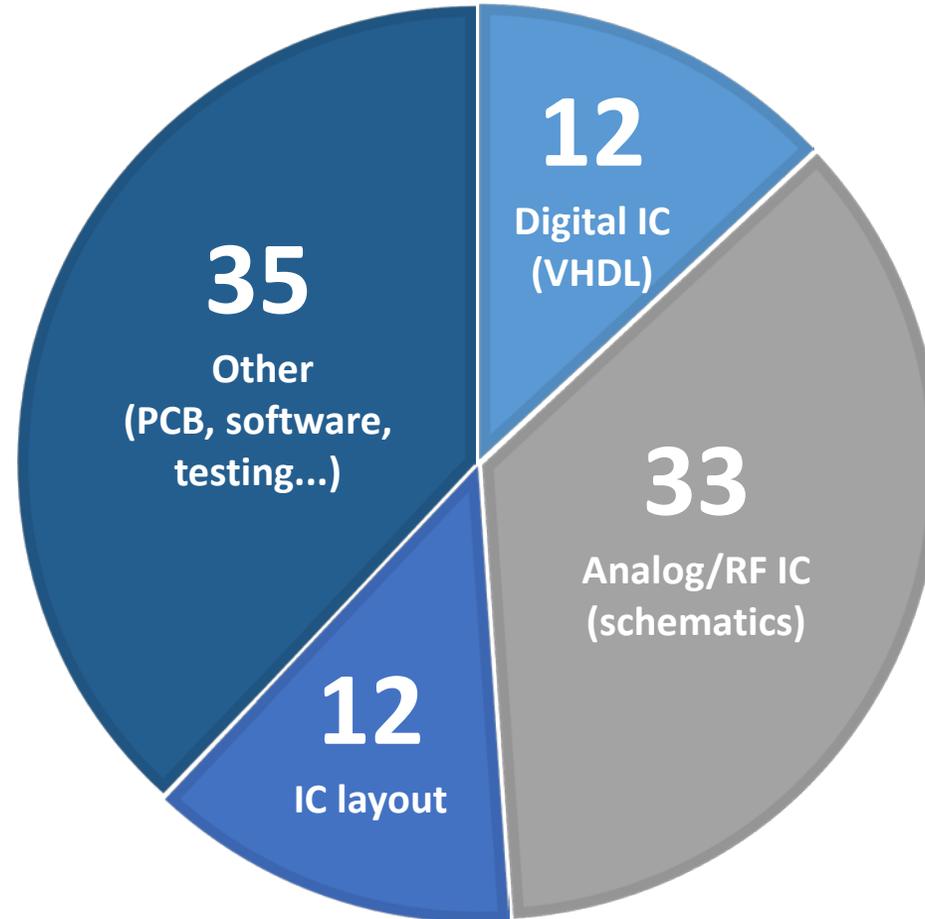


Off-the-shelf IPs



IP porting & modification

Engineering personnel



Company staff: 146 employees

Company milestones

1989

1994

1998

2000

2006

2015

2016

2018

1989: Company started in the field of RISC architecture

1994: Project with EU Space Agency (satellite angle measurement)

1998: RF development started: automotive ASICs for Melexis (Belgium)

2000: GNSS development started with Russian Federal Navigation program

2006: NFC and RFID development started: Biometric Russian Passport and
MIR Universal ID/Payment card

2015: Medical development started: 'Narcine'– neurostimulation implant

2016: First commercial ASIC product: NT1065 'Nomada'

2018: Professional audio: front-end processor development

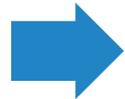
And in 2019 we have....

Company achievements



24 ASICs

For communication systems



19 ASICs

In satellite GNSS navigation



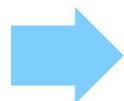
9 ASICs, 3 IPs

In UHF RFID and NFC area



2 ASICs

For medical applications



>400 IPs

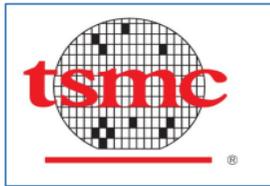
For different purposes: ADC, DAC, PLL, PMU, RF, Interfaces



11 NTLab's own products

ASICs

Semiconductor technologies



28nm MS

40nm

55/65nm RF

90nm RF

130nm MS

180nm SiGe RF



65nm CMOS



40nm RF

55nm RF

65nm RF

180nm BCD



55nm RF

180nm MS



28nm FD-SOI



130nm SiGe

250nm SiGe



180nm XH

350nm RF

600nm SiGe



55nm RF

180nm SiGe

180nm PM SOI



90nm

180nm RF



180nm MS/RF



150nm GaAs pHEMT

500nm GaAs

500nm GaAs pHEMT



350nm SiGe



250nm MS/RF

350nm MS/RF

500nm MS/RF

Spheres of design



RFID/NFC



GNSS navigation



Internet of Things



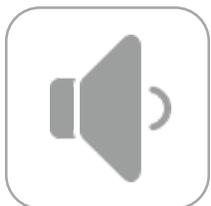
**Narrow & Wideband
communication systems**



**Medical implantable
applications**

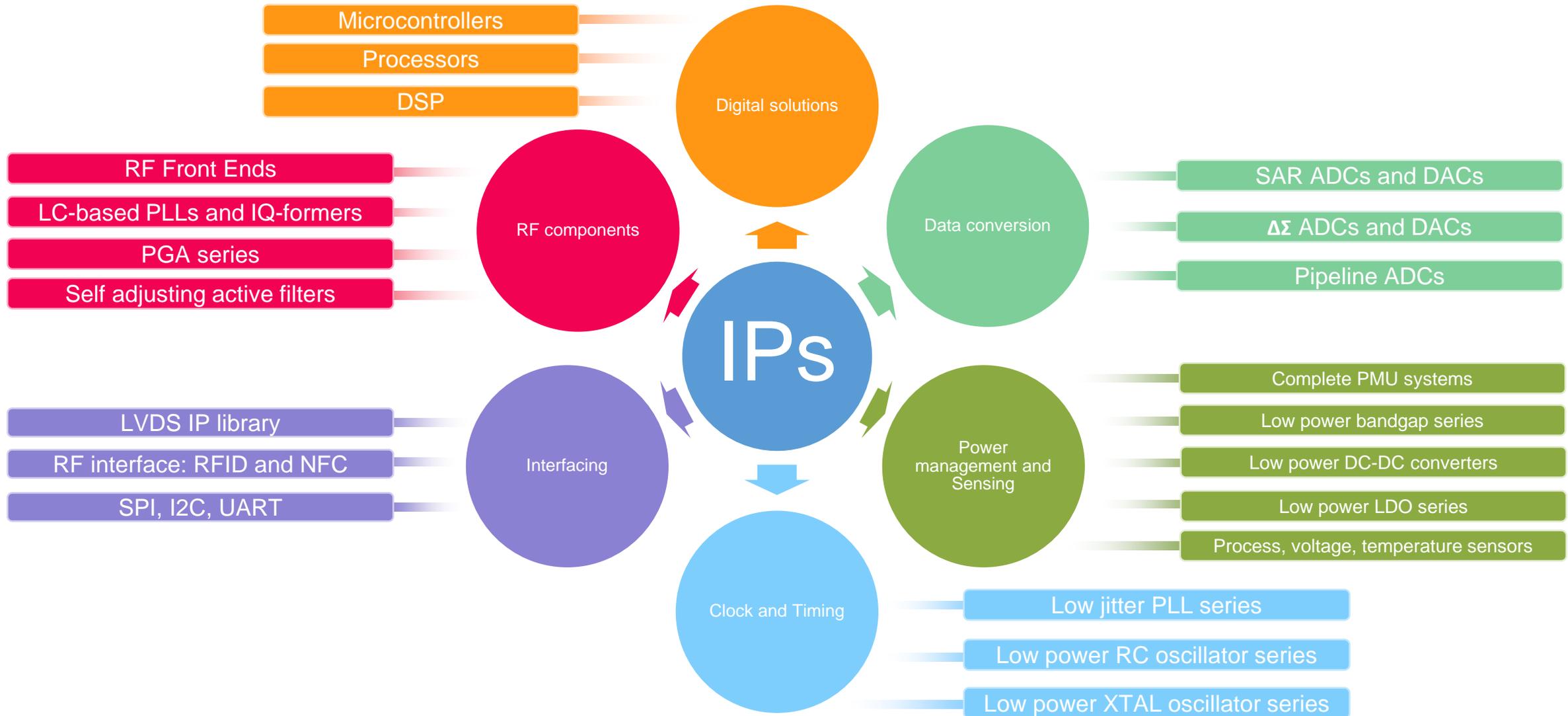


Automotive applications



Professional audio

IP range



Digital solutions

Dual-core microcontroller

- Two 32-bit CPU with FP and caches
- Operating frequency: 450 MHz
- Video controller
- DDRAM controller
- USB 2.0 interface
- Number of gates: 970K
- TSMC CMOS 90nm

GNSS processor

- 64-channel complex correlator
- Operating frequency: 200 MHz
- 32 bit CPU with FP
- 1 MByte SRAM
- Number of gates: 2983K
- TSMC LP 65nm

Beamforming processor

- Four 7-channel complex auto compensation units
- Two 8-channel high speed ADC interfaces
- 32-bit CPU
- Operating frequency: 100 MHz
- Number of gates: 4582K
- TSMC LP 65nm

FSK demodulator

- Compatible with 12-bit $\Delta\Sigma$ ADC
- Pre-filtering on CIC decimator and FIR
- CORDIC-based demodulation
- Received data bitrate: 0.1 ... 200Kbps
- Number of gates: 65K
- UMC eFlash CMOS 55nm

Data conversion IPs: $\Delta\Sigma$ ADCs

12-bit switched capacitor cascade 2-2
low power $\Delta\Sigma$ ADC

- Bandwidth: 150kHz
- SINAD: 70dB
- SFDR: 78dB
- ENOB: 11.3bit
- OSR: 16
- Supply voltage: 1.2V, I_{cc} : 0.3mA
- TSMC CMOS 65nm

24-bit switched capacitor cascade 2-2
high performance $\Delta\Sigma$ ADC

- Bandwidth: 20kHz
- SINAD: 114dB
- SFDR: 118dB
- ENOB: 19bit
- OSR: 256
- Supply voltage: 5V, I_{cc} : 30mA
- Tower Jazz 180nm PM SOI

Data conversion IPs: SAR ADCs

12-bit low power SAR ADC

- Sample rate: 2k ... 1MSPS
- DNL: $\pm 1.1\text{LSB}$, INL: $\pm 3.3\text{LSB}$
- SINAD: 63dB @ 1MSPS
- ENOB: 10.2bit @ 1MSPS
- Supply voltage: 1.8V/3.3V
- Power consumption: 148uW @ 1MSPS, 1.8V
- TSMC Flash ULP 40nm

12-bit single-ended SAR ADC

- Sample rate: 20 ... 200 kSPS
- DNL: $\pm 0.16\text{LSB}$, INL: $\pm 0.45\text{LSB}$
- SINAD: 70.9dB @ 200kSPS
- ENOB: 11.5bits @ 200kSPS
- Supply voltage: 1.2V + 3.0V
- Power consumption: 133uW @ 200kSPS
- UMC eFlash CMOS 55nm

14-bit SAR ADC

- Sample rate: 0.2 ... 1MSPS
- DNL: $\pm 0.1\text{LSB}$, INL: $\pm 0.4\text{LSB}$
- SFDR: 80dB
- ENOB: 12 bit
- Supply voltage: 1.2V + 2.5V
- Power consumption: 11mW @ 1MSPS
- STM CMOS 65nm

Data conversion IPs: pipeline ADCs

12-bit pipeline ADC

- Sample rate: 50/100/125MSPS
- Bandwidth: 510MHz
- SINAD: 59.5/59/58dB @ 50/100/125MSPS
- SFDR: 73.7/73.4/70.8dB @ 50/100/125MSPS
- ENOB: 9.6/9.5/9.4bit @ 50/100/125MSPS
- Supply voltage: 1.2V
- Power consumption: 41/61/71mW @ 50/100/125MSPS
- TSMC CMOS 65nm

14-bit pipeline ADC

- Sample rate: 50MSPS
- Bandwidth: 300MHz
- SINAD: 63.8dB
- SFDR: 77dB
- ENOB: 10.3bit
- Supply voltage: 1V + 1.8V
- Power consumption: 170mW
- TSMC MS CMOS 90nm

Data conversion IPs: DACs

12-bit current-steering DAC

- Sample rate: 10 ... 150MSPS
- SFDR: 77.1/75.7/74.0dB @ 50/100/150MSPS
- DNL: ± 1.27 LSB
- INL: ± 2.0 LSB
- Supply voltage: 2.0 ... 2.5V
- Power consumption: 42/47/51mW @ 50/100/150MSPS
- TSMC CMOS 55nm

14-bit high-performance current-steering DAC

- Sample rate: 40 ... 500MSPS
- SFDR: 83.8dB @ 500MSPS
- DNL: ± 0.5 LSB
- INL: ± 1 LSB
- Supply voltage: 1.2V + 2.5V
- Power consumption: 60mW @ 500MSPS
- STM CMOS 65nm

16-bit $\Delta\Sigma$ DAC

- Sample rate: 50kSPS
- SNR: 69dB
- SFDR: 83dB
- OSR: 512
- Supply voltage: 1.8V + 3.0V
- Power consumption: 30mW
- TSMC SiGe BiCMOS 180nm

14-bit R-2R DAC

- Sample rate: 1MSPS
- SFDR: 95dB
- DNL: ± 1 LSB
- INL: ± 2 LSB
- Supply voltage: 1.2V + 2.5V
- Power consumption: 8mW
- STM CMOS 65nm

Power management IPs

Complete PMU system

- Input voltage: 2.0 ... 3.6V
- Four LDOs: 2x1.2V, 1.6V, 2V
- Output voltage trimming
- Output reference voltage : 650mV
- Output reference currents: 1 μ A, 40nA
- Quiescent current: 75 μ A
- UMC eFlash CMOS 55nm

Low power bandgap voltage reference

- Input voltage: 2.0 ... 3.6V
- Output voltage: 0.65V
- Output voltage variation: 3%
- Quiescent current: 0.23 μ A
- UMC eFlash CMOS 55nm

Ultra low power LDO voltage regulator

- Input voltage: 1.6V ... 3.6V
- Output voltage: 0.4V ... 0.9V
- Voltage step: 7.9mV
- Maximum load: 0.01 1mA
- Quiescent current: 17.5nA
- TSMC Flash ULP 40nm

Low power bandgap voltage reference

- Input voltage: 0.8V ... 1.8V
- Output voltage: 0.4V
- Output voltage accuracy: 1%
- Quiescent current: 0.5 μ A
- Samsung FD-SOI 28nm

Power management IPs

DC-DC step-down converter

- Input voltage: 2.0 ... 3.6V
- Output voltage: 1.2V
- Power conversion efficiency: 89%
- Quiescent current: 0.3mA @ $I_{out}=50\text{mA}$
- UMC eFlash CMOS 55nm

DC-DC step-up converter

- Input voltage: 2.7V
- Output voltage: 2.7/2.8/2.9/3.0V
- Power conversion efficiency: 90% @ 3.0V output
- Quiescent current: 10mA @ $I_{out}=250\text{mA}$
- iHP SiGe BiCMOS 130nm

Process/voltage/temperature sensor

- Voltage measurement range: 0.8V ... 1.35V, 2.4V ... 3.7V
- Voltage measurement accuracy: $\pm 2\%$ with trimming
- Temperature measurement range: $-40\text{ }^{\circ}\text{C}$... $+125\text{ }^{\circ}\text{C}$
- Temperature measurement accuracy: $\pm 2\text{ }^{\circ}\text{C}$ with trimming
- NMOS and PMOS transistors set and metal stack for process monitoring
- Output data resolution: 10bit
- TSMC CMOS 28nm

Clock and timing IPs

Ultra low power crystal oscillator

- Output frequency: 32.768kHz
- Accuracy: 0.1%
- I_{cc}: 0.25uA
- UMC eFlash CMOS 55nm

Ultra low power RC oscillator

- Output frequency: 3.2MHz
- Output frequency calibration
- Accuracy: 4.3%
- I_{cc}: 0.3uA
- TSMC Flash ULP 40nm

XTAL oscillator

- Frequency range: 10 ... 50 MHz
- Phase noise @50MHz:
 - 108dBc/Hz @ 10Hz offset
 - 140dBc/Hz @ 10kHz offset
- Tower Jazz 180nm PM SOI

Clock and timing IPs

LC-based PLL frequency synthesizer

- Frequency range: 50 ... 7000 MHz
- RMS jitter: down to 0.3ps
- Built-in GFSK modulator
- TSMC CMOS 55nm

DLL-based frequency multiplier

- Input frequency range: 0.01 ... 100 MHz
- Output frequency range: 2.5 ... 200 MHz
- Output frequency jitter: 0.3ns @ 200MHz
- GF CMOS 55nm

Ring PLL for digital circuit clocking

- Frequency range: 50 ... 800 MHz
- Phase noise: -97dBc/Hz @1MHz
- TSMC CMOS 65nm

Data interfacing IPs

LVDS RX/TX IP library including:

- Transmitter LVDS driver
- Receiver LVDS driver
- Transceiver LVDS driver
- Reference voltage and current source

Features:

- TIA/EIA-644 LVDS standards without hysteresis
- Composition of up to 16 pairs of data channels and 2 pairs of synchronization channels
- 200 Mbps (DDR MODE) data rates per channel
- 3.3V IO voltage supply
- 1.8V core voltage supply
- 1.8V CMOS input/output logic control signals
- Embedded 1.8V/3.3V level shifters
- TSMC 180nm GP CMOS

RFID & NFC IPs

13.56MHz field-powered RFID tag IP

- Passive mode (zero consumption from battery, fully field-powered)
- ISO14443 A/B contactless interface
- Cryptographic coprocessors: GOST, DES, AES, ECDSA, RSA

NFC Interface IP

- NFC-reader mode and NFC-tag emulation mode
- Pear-to-pear support
- Optional embedded MCU for NFC protocol

UHF EPC Gen2 Air Interface IP

- Input frequency: 860 ... 960MHz
- Energy harvesting from RF field
- EPC Gen2 V2 v2.0.1, ISO / IEC 18000-63 compliant

RF components IPs

Low noise amplifier

- Operating frequency: 25 ... 1750MHz
- Gain: 20dB
- Noise figure: 1.0dB
- IP1dB: -20dBm
- IIP3: -15dBm
- TSMC CMOS 55nm

High linearity low noise amplifier

- Operating frequency: 1550 ... 2500MHz
- Gain: 20dB
- Noise figure: 1.7dB
- IP1dB: -11.5dBm
- IIP3: 7.7dBm
- TSMC SiGe BiCMOS 180nm

A class power amplifier

- Operating frequency: 75 ... 3000MHz
- Maximum output power: +8dBm
- TSMC CMOS 65nm

AB class power amplifier

- Operating frequency: 8000 ... 12000MHz
- Maximum output power: +4dBm
- TSMC CMOS 55nm

E class power amplifier

- Operating frequency: 3000 ... 5000MHz
- Maximum output power: +8dBm
- iHP SiGe BiCMOS 130nm

RF components IPs

Quadrature mixer

- Input frequency: 25 ... 1750MHz
- Output frequency: 2.4 ... 3000kHz
- Gain: -1.5dB
- Noise figure: 7.5dB
- IP1dB: -14.6dBm
- IIP3: 4.5dBm
- TSMC CMOS 55nm

High linearity mixer

- Input frequency: 1150 ... 2500MHz
- Output frequency: 2 ... 100MHz
- Gain: 0dB
- Noise figure: 13dB
- IP1dB: 3.2dBm
- IIP3: 10.5dBm
- TSMC SiGe BiCMOS 180nm

Quadrature mixer

- Input frequency: 500 ... 1500MHz
- Bandwidth: 35MHz
- Gain: -1dB
- Noise figure: 14.5dB
- IP1dB: -2.4dBm
- IIP3: 6.7dBm
- TSMC SiGe BiCMOS 180nm

Image rejection mixer

- Input frequency: 1150 ... 1620MHz
- Output frequency: 2 ... 100MHz
- Image rejection: 30dB
- Gain: 25dB
- TSMC SiGe BiCMOS 180nm

RF components IPs

IF amplifier&filter

- Operating frequency: 0.5 ... 36MHz
- AGC range: 50dB
- Gain: 54dB max, 4dB min
- Gain step: 1dB
- Noise figure: 12dB @ 54dB gain
- Cut-off frequency: 36MHz max, 1.5MHz min
- TSMC CMOS 55nm

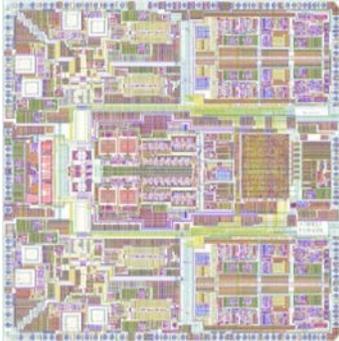
Programmable gain amplifier

- Operating frequency: 0.05 ... 10MHz
- AGC range: 76dB
- Gain: 70dB max, -6dB min
- Noise figure: 20dB
- TSMC SiGe BiCMOS 180nm

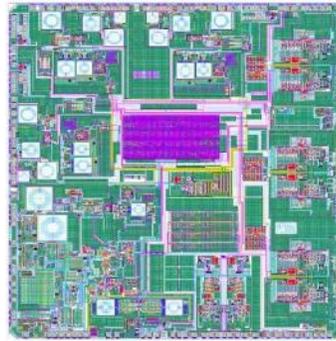
High linearity PGA

- Operating frequency: 2 ... 50MHz
- AGC range: 46.1dB
- Gain: 47.9dB max, 1.8dB min
- Gain step: 0.73dB
- Noise figure: 7.7dB @ 47.9dB gain
- OP1dB: 12dBm
- OIP3: 36.3dBm @ $V_{out}=2V_{p-p}$
- TSMC SiGe BiCMOS 180nm

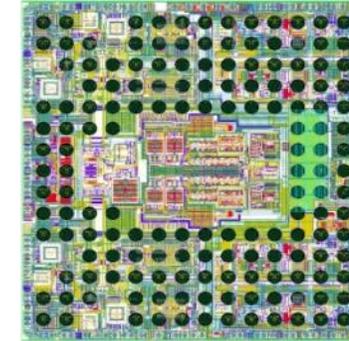
Own products: 4-channel RF Front-End ICs for GNSS



- ❑ 4-Channels RF FE IC, 2 PLL or 1 PLL modes
- ❑ GPS/GLONASS/Galileo/BeiDou/NavIC/QZSS
- ❑ L1/L2/L3/L5/E1/E5/E6/B1/B2/B3
- ❑ QFN88 package



- ❑ 4-Channels RF FE IC, 4 PLL mode
- ❑ GPS/GLONASS/Galileo/BeiDou/NavIC/QZSS
- ❑ S/L1/L2/L3/L5/E1/E5/E6/B1/B2/B3
- ❑ Software-reconfigured to receive real-time corrections data transmitted over FM, VHF and UHF bands
- ❑ QFN108 package

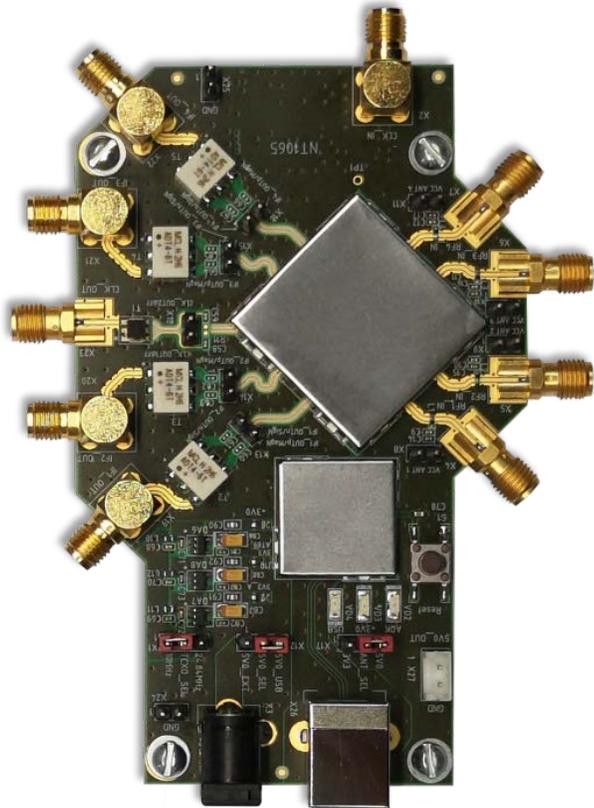


- ❑ 4-Channel RF FE IC, 2 PLL or 1 PLL modes
- ❑ GPS/GLONASS/Galileo/BeiDou/NavIC/QZSS
- ❑ S/L1/L2/L3/L5/E1/E5/E6/B1/B2/B3
- ❑ WLCSP or QFN88 packages

Evaluation kits for RF ASICs

NT1065_EVK

- SMA RF inputs
- PLD / SMA IF outputs
- Analog / 2-bit ADCs outputs



NT1065_FMC

- SMA RF inputs
- FMC connector
- 2-bit /12-bit /14-bit ADCs outputs



NT1065_USB3

- SMA RF inputs
- USB3.0 output
- Raw data output



THANKS FOR YOUR ATTENTION!



www.ntlab.com



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