MOVELLUS

ANALOG GONE DIGITAL™

High Performance PLL - Customizable in Weeks

Movellus' high-performance PLLs are implemented using our proprietary technology resulting in the smallest area in the industry for a given application and process node. Boasting higher reliability and fully SCAN enabled, this PLL can be customized in weeks, allowing SoC architects to specify the features they need and/or request new features in order to improve the overall performance of their chip.

Key Features

- Fully SCAN enabled
- Fully customizable to each application
- Wide operating voltages available for DVFS (e.g. 0.58V to 0.93V in N7)
- Multiple output phases for di/dt smearing
- Integrated LDO
- Low jitter
- Smallest area in the industry
- Integer or fractional division
- Maximum 8 metal layers
- JTAG and APB programing
- Simple integration
- Portable to any process and available in TSMC 7nm

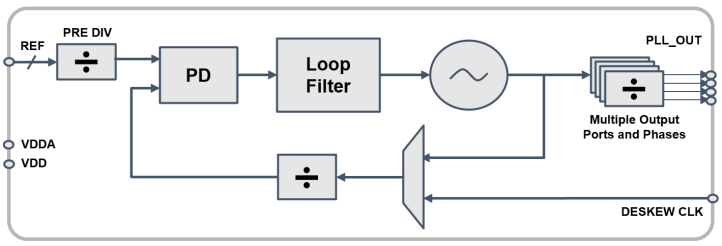
Sample Applications

- Cloud AI
- Multi-core processors
- Graphics
- Networking

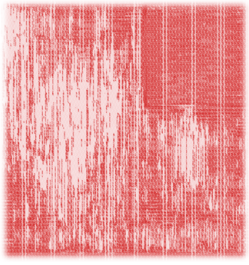
Specifications Range

Input Frequency	32kHz – 100MHz
Input Clocks	1-4
Output Frequency	4MHz - 6GHz
Output Clocks	1-4
Output Phases	1-8
Period Jitter	NDA
Lock Time	500 ref clk cycles
Area	NDA
Power	800uW - 10mW*
Fractional Bits	2-24
Divider Range	1-256
Supply	Core VDD / 1.2-1.8V
Temperature	-40C to 125C

** See Movellus' ULPDPLL / LPDPLL product briefs for lower power*



HPDPLL Block Diagram



GDS Example

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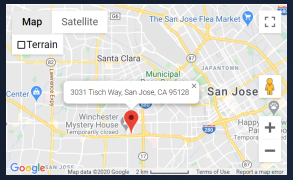

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