MOVELLUS

ANALOG GONE DIGITAL™

Low Power PLL - Customizable in Weeks

*Movellus' low power PLLs are implemented using our proprietary technology resulting in the **smallest area and lowest power** in the industry for a given application and process node. All Movellus PLLs can be customized for your specific application within weeks and are the only PLLs available that are SCAN enabled.*

Key Features

- Lowest power in the industry
- Smallest area in the industry
- Customizable in weeks
- 0 ppm frequency error for audio applications
- Integer or fractional division
- Low voltage operation available
- Maximum 8 metal layers
- Fully SCAN enabled
- JTAG and APB programing
- Simple integration
- Portable to any process and available in GF, TSMC, UMC and Fujitsu processes from 40nm to 22nm

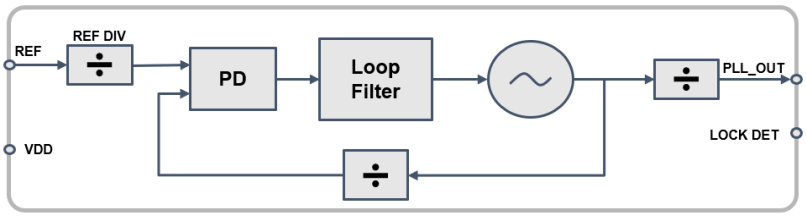
Sample Applications

- Edge AI Neural Processing
- IoT / Sensors
- Wireless
- Audio DAC and ADC clocking

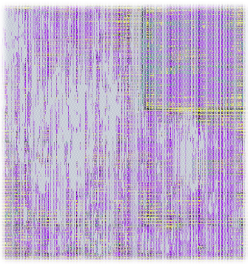
Specifications Range

Input Frequency	32kHz – 100MHz
Input Clocks	1-4
Output Frequency	100kHz - 1GHz*
Output Clocks	1-8
Period Jitter	NDA
Lock Time	500 ref clk cycles
Area	NDA
Power	0.5 - 1.5mW**
Fractional Bits	2-24
Divider Range	1-256
Supply	Core VDD
Temperature	-40C to 125C

** See Movellus' HPDPLL product brief for higher performance*
*** See Movellus' ULPDPLL product brief for lower power*



LPDPLL Block Diagram



GDS Example

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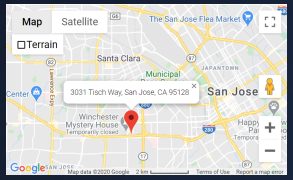

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