

### UMC40 Ultra-Low Power PLL - Customizable in Weeks

Movellus' ultra-low power PLLs are implemented using our proprietary technology, resulting in the smallest area in the industry for a given application and process node. Designed for higher reliability and fully SCAN enabled, all our PLLs can be customized in weeks, allowing SoC architects to specify the features they need and/or request new features in order to improve the overall performance of their chip.

#### Product Specifications

|                      |                   |
|----------------------|-------------------|
| Input Frequency      | 8kHz – 4MHz       |
| Input Clocks         | 1                 |
| Output Frequency     | 14MHz - 126MHz    |
| Output Clocks        | 1                 |
| Period Jitter (rms)  | NDA*              |
| Duty Cycle           | 45% / 55%         |
| Phase Lock Time      | 750 refclk cycles |
| Area                 | NDA*              |
| Power                | NDA*              |
| Feedback Division    | 3b Fractional     |
| Input Divider Range  | 1 – 16            |
| Output Divider Range | 1 – 16            |
| APB Frequency        | 50MHz             |
| JTAG Frequency       | 50MHz             |
| SCAN Frequency       | 50MHz             |

\* Will be disclosed upon signing an NDA

#### Process Specifications

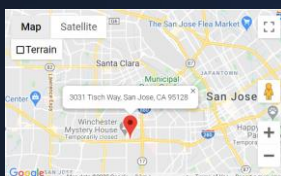
|                    |               |
|--------------------|---------------|
| Process Technology | UMC40         |
| Metal Stack        | 1P7M0T1U      |
| Top-level Metal    | M5            |
| VDD                | 0.81V – 1.21V |
| Temperature        | -40C to 125C  |
| Transistors        | eHVT          |

#### Optional Customizations

|                     |                                       |
|---------------------|---------------------------------------|
| Post-dividers       | Fixed or programmable division ranges |
| Output clocks       | Synchronization, Multiple phases      |
| SSC                 | Frequency spread, rate                |
| Fractional feedback | 0b – 24b (minimal impact on power)    |
| Lock Detection      | Frequency and/or phase                |
| DVFS                | Frequency transition rates            |



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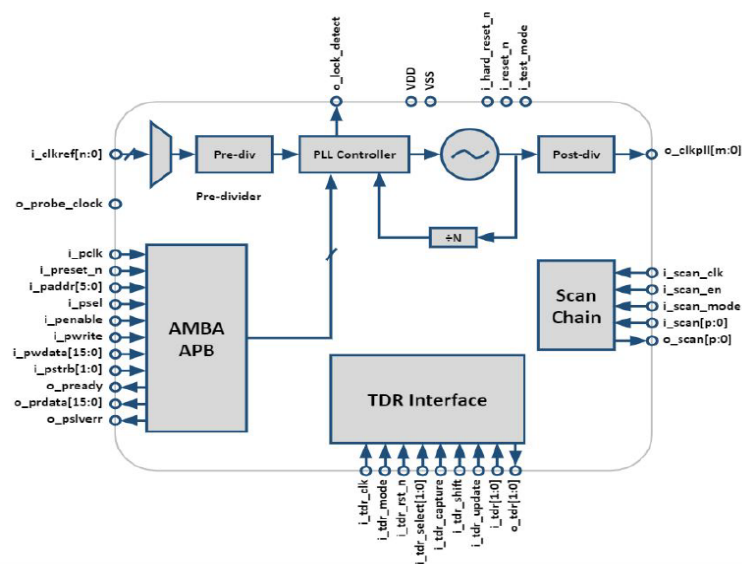
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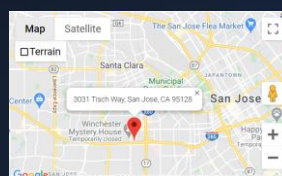
## Deliverables

|                     |                       |
|---------------------|-----------------------|
| User's Guide        | Usage and integration |
| IPXACT              | Register Map          |
| Verilog Model       | Verilog simulation    |
| Verilog Testbenches | IP Usage              |
| Gate-level Netlist  | DFT/SCAN testing      |
| LEF                 | Floorplanning         |
| LIB                 | Timing models         |
| GDS                 | Physical Integration  |
| CDL netlist         | LVS                   |

## Block Diagram



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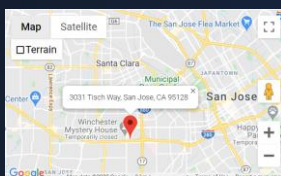
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## Pin Descriptions

| <u>Pin Name</u>   | <u>Direction</u> | <u>Description</u>  |
|-------------------|------------------|---|
| VDD               | Supply           | Power supply  |
| VSS               | Supply           | Ground  |
| i_hard_reset_n    | Input            | Hard master reset   |
| i_reset_n         | Input            | Reset   |
| i_clkref[n:0]     | Input            | Low frequency reference clock(s)                              |
| o_clkpll[m:0]     | Input            | High frequency output clock(s)                                |
| o_lock_detect     | Input            | Indicates PLL frequency and phase lock                        |
| i_test_mode       | Input            | Activates PLL test mode                                       |
| i_preset_n        | Input            | APB bus reset   |
| i_pclk            | Input            | APB bus clock   |
| i_paddr[5:0]      | Input            | APB bus address   |
| i_psel            | Input            | APB bus select  |
| i_penable         | Input            | APB bus enable  |
| i_pwrite          | Input            | APB bus transfer direction                                    |
| i_pwdata[15:0]    | Input            | APB bus write data  |
| i_pstrb[1:0]      | Input            | APB bus strobe  |
| o_prdata[15:0]    | Output           | APB bus read data   |
| o_pready          | Output           | APB bus slave ready   |
| o_pslverr         | Output           | APB bus transfer error  |
| i_tdr_mode        | Input            | Selection of TDR vs. APB registers for transfer into PLL core |
| i_tdr_clk         | Input            | TDR bus clock   |
| i_tdr_rst_n       | Input            | TDR bus reset   |
| i_tdr_select[1:0] | Input            | TDR bus chain selection                                       |
| i_tdr_capture     | Input            | TDR bus capture   |
| i_tdr_shift       | Input            | TDR bus shift   |
| i_tdr_update      | Input            | TDR bus update  |
| i_tdr[1:0]        | Input            | TDR bus input data  |
| o_tdr[1:0]        | Output           | TDR bus output data   |
| o_probe_clock     | Output           | Test clock  |
| i_scan_clk        | Input            | SCAN bus clock  |
| i_scan_en         | Input            | SCAN bus enable   |
| i_scan_mode       | Input            | SCAN bus mode   |
| i_scan[p:0]       | Input            | SCAN bus input  |
| o_scan[p:0]       | Output           | SCAN bus output   |



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