MOVELLUS

Application-Optimized IP™

GF12LP Low Power PLL - Customizable in Weeks

Movellus' low power PLLs are implemented using our proprietary technology, resulting in the smallest area in the industry for a given application and process node. Designed for higher reliability and fully SCAN enabled, all our PLLs can be customized in weeks, allowing SoC architects to specify the features they need and/or request new features in order to improve the overall performance of their chip.

Product Specifications

Input Frequency	26MHz – 100MHz
Input Clocks	1
Output Frequency	5.9MHz – 3GHz
Output Clocks	4
Period Jitter (P-P)	NDA*
Duty Cycle	49 / 51 %
Frequency Lock	100 refclk cycles
Area	NDA*
Power	NDA*
Feedback Division	8b Fractional
Input Divider Range	1 – 1023
Output Divider Range	1 – 255
APB Frequency	120MHz
JTAG Frequency	100MHz
SCAN Frequency	50MHz

** Will be disclosed upon signing an NDA*

Process Specifications

Process Technology	GF12LP
Metal Stack	3Mx_2Cx_4Kx
Top-level Metal	M8
VDD	0.8V
VDDA	0.8V
Temperature	-40C to 125C
Transistors	sLVT / LVT / SVT

Optional Customizations

Post-dividers	Fixed or programmable division ranges
Output clocks	Synchronization, Multiple phases
SSC	Frequency spread, rate
Fractional feedback	0b – 24b (minimal impact on power)
Lock Detection	Frequency and/or phase
DVFS	Frequency transition rates

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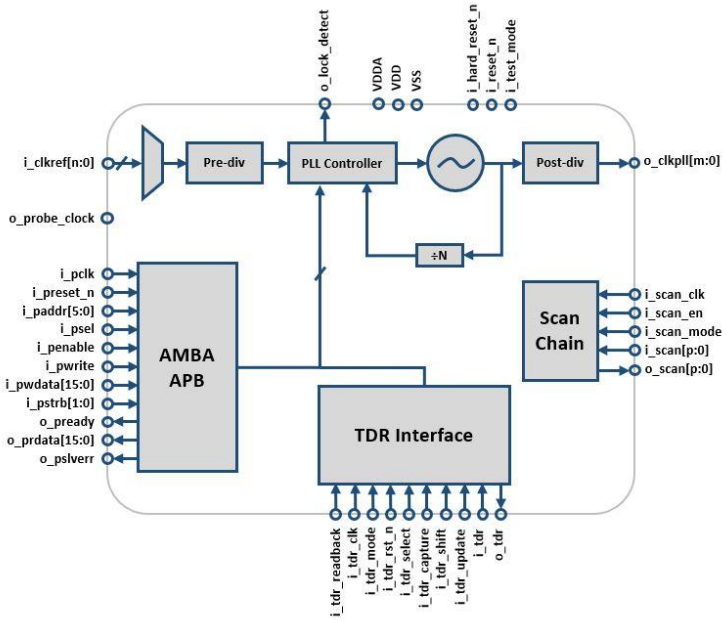
Deliverables

User's Guide	Usage and integration
IPXACT	Register Map
Verilog Model	Verilog simulation
Verilog Testbenches	IP Usage
Gate-level Netlist	DFT/SCAN testing
LEF	Floorplanning
LIB	Timing models
GDS	Physical Integration
CDL netlist	LVS

Block Diagram



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Pin Descriptions

Pin Name	Direction	Description
VDD	Supply	Core power supply
VDDA	Supply	Quiet power supply
VSS	Supply	Ground
i_hard_reset_n	Input	Hard master reset
i_reset_n	Input	Reset
i_clkref[n:0]	Input	Low frequency reference clock(s)
o_clkpll[m:0]	Input	High frequency output clock(s)
o_lock_detect	Input	Phase lock indicator
i_preset_n	Input	APB bus reset
i_pclk	Input	APB bus clock
i_paddr[5:0]	Input	APB bus address
i_psel	Input	APB bus select
i_penable	Input	APB bus enable
i_pwrite	Input	APB bus transfer direction
i_pwdata[15:0]	Input	APB bus write data
i_pstrb[1:0]	Input	APB bus strobe
o_prdata[15:0]	Output	APB bus read data
o_pready	Output	APB bus slave ready
o_pslverr	Output	APB bus transfer error
i_tdr_readback	Input	TDR register readback selection
i_tdr_mode	Input	TDR register pin override
i_tdr_clk	Input	TDR bus clock
i_tdr_rst_n	Input	TDR bus reset
i_tdr_select	Input	TDR bus chain selection
i_tdr_capture	Input	TDR bus capture
i_tdr_shift	Input	TDR bus shift
i_tdr_update	Input	TDR bus update
i_tdr	Input	TDR bus input data
o_tdr	Output	TDR bus output data
o_probe_clock	Output	Test clock
o_probe_analog	Output	Analog test port
i_test_mode	Input	Test mode selection
i_scan_clk	Input	SCAN bus clock
i_scan_en	Input	SCAN bus enable
i_scan_mode	Input	SCAN bus mode
i_scan[p:0]	Input	SCAN bus input
o_scan[p:0]	Output	SCAN bus output

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