COMPANY PROFILE

STRUENT SEMICONDUCTORS

We Build Silicon

"We Build Silicon"

In Latin, "Struent" means "to build". True to our name, our mission is to build exceptional products and deliver significant value to our clients.

To build high-Quality Silicon

Established 29-May-2021

Headquarters Chennai

Privately owned and funded

CIN U72900TN2021PTC143785

https://struentsemi.com

Why Us

Domain expertise, established workflows, and automation backed by an Experienced team with lot of success stories

What we do

We engage with customers to build their silicon product/systems through our expertise and innovation

How we do

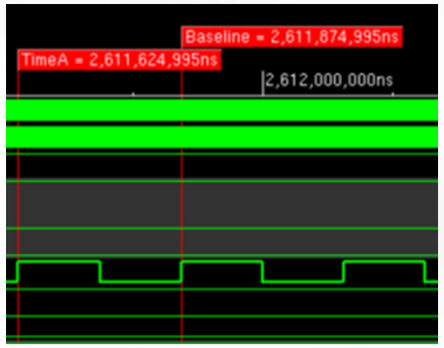
Through Various business models, we provide Spec2GDSII services, and eventually spec2parts.

SERVICE OFFERING - TRADITIONAL SERVICES

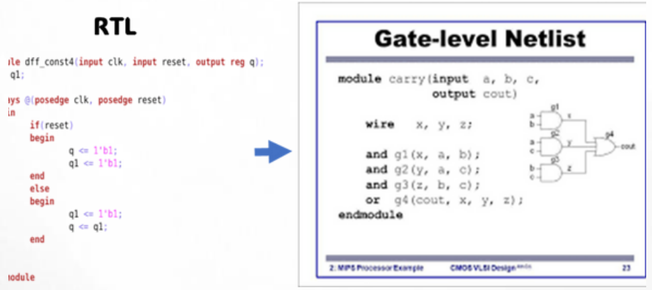
RTL DESIGN

```
architecture Behavioral of Button2 is
   signal Q:     STD_LOGIC_VECTOR( 1 to 4);
   signal Sreg: STD_LOGIC_VECTOR( 1 downto 0):= "00";

   constant S0: STD_LOGIC_VECTOR( 1 downto 0):= "00";
   constant S1: STD_LOGIC_VECTOR( 1 downto 0):= "11";
   constant S2: STD_LOGIC_VECTOR( 1 downto 0):= "10";
   signal Set,Res: STD_LOGIC;
begin

   Set <= '1' when Q="1111" else '0';
   Res <= '1' when Q="0000" else '0';

   --------------Implements a 4-bit shiftregister -----
   process( Clk)
   begin
      if Rising_edge(Clk) then
         Q <= Q(2 to 4)& Button;
      end if;
   end process;
   -------------- State Machine -----------------------
   -- Q(1) Coded as a debounced Button signal
   -- Q(0) Coded as a pulse bit - One clock pulse wide
```

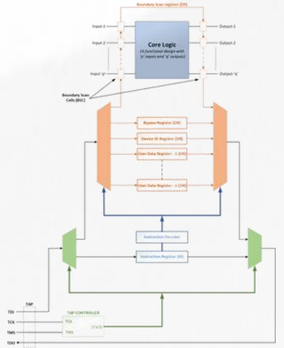
DESIGN VERIFICATION



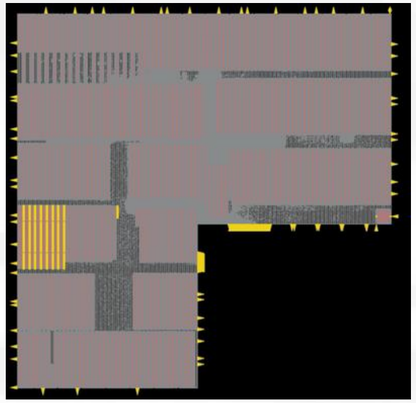
SYNTHESIS



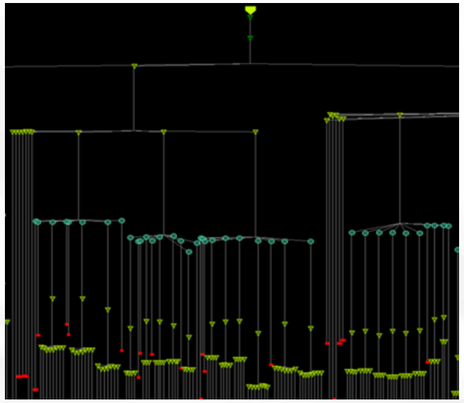
DESIGN FOR TEST



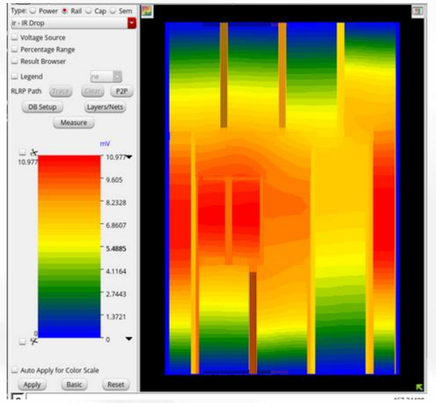
PHYSICAL DESIGN



STATIC TIMING ANALYSIS



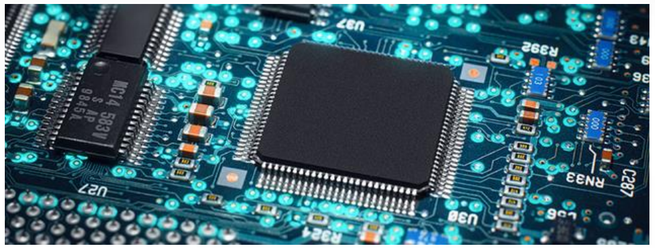
IR ANALYSIS



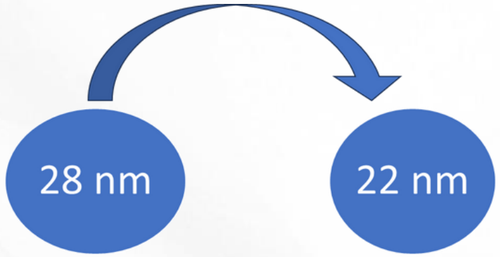
PHYSICAL VERIFICATION

SERVICE OFFERING - CUSTOMIZED SERVICES

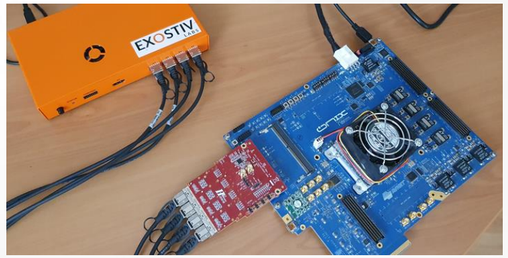
IP HARDENING



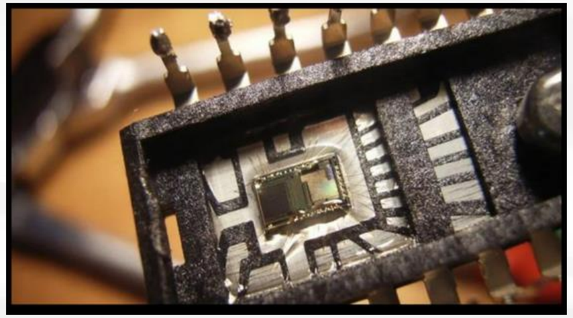
TECHNOLOGY MIGRATION



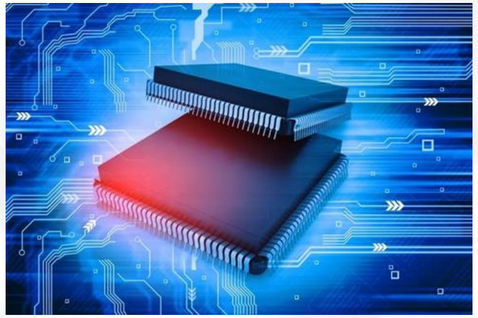
FPGA PROTOTYPING



OLDER NODE IMPLEMENTATION



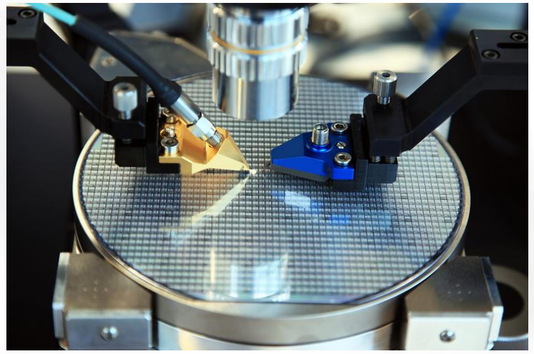
DERIVATIVE CHIP IMPLEMENTATION



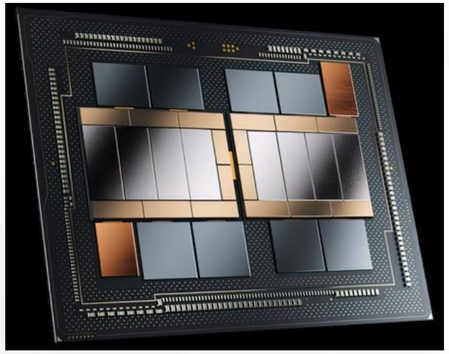
POST-SILICON VALIDATION

SERVICE OFFERING - ADVANCED SERVICES

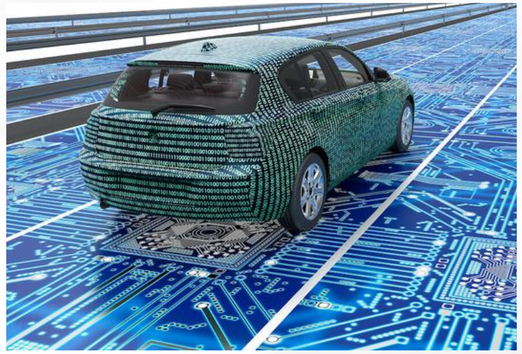
TESTCHIP IMPLEMENTATION - MPW (VCA)



CHIPLETS

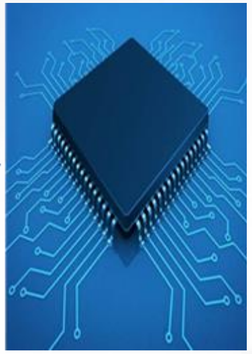


AUTOMOTIVE CHIP COMPLIANCE



SPEC2PARTS

SPECIFICATIONS	
TECH NODE	22nm
FREQUENCY	1GHZ
NO. OF BLOCKS	2

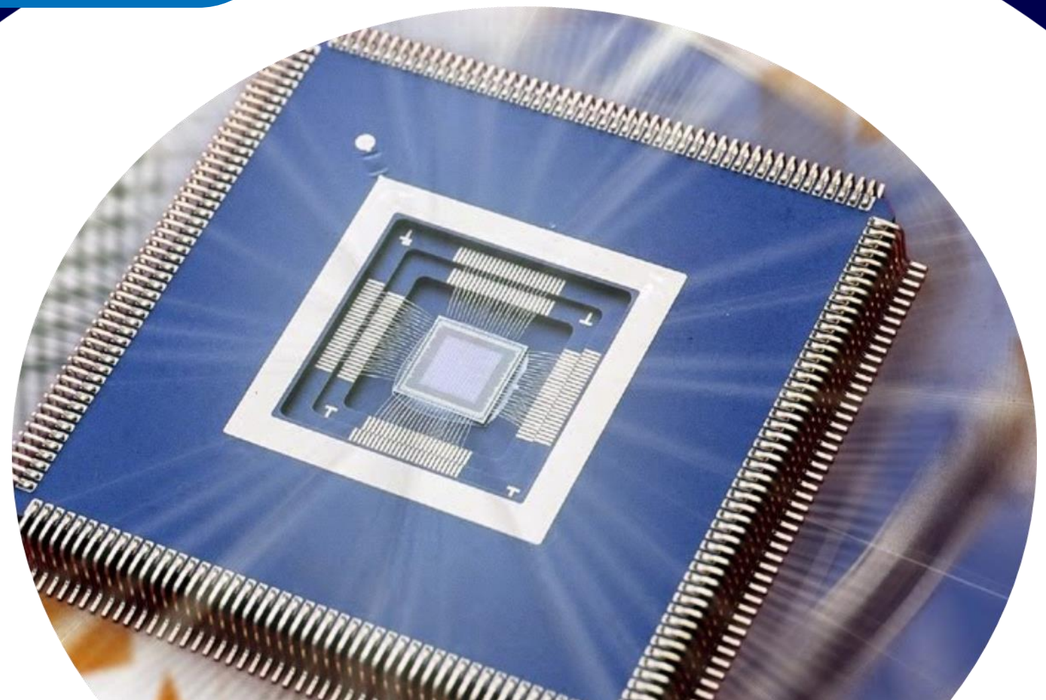


Analog IP

We deliver/support the following IP’s

A/D Converter IP

SERDES IP



Sub - GHz Transceiver IP

Clock & Power IP

Spec2GDSII Expertise

- Architecture Definition
- Micro-architecture & block Diagram
- RTL Design
- Design Verification
- Synthesis
- DFT
- P&R
- STA
- IR Analysis
- Physical Verification

FOUNDRIES

UMC
TILL 22nm

TSMC
TILL 7nm

Samsung
TILL 5nm

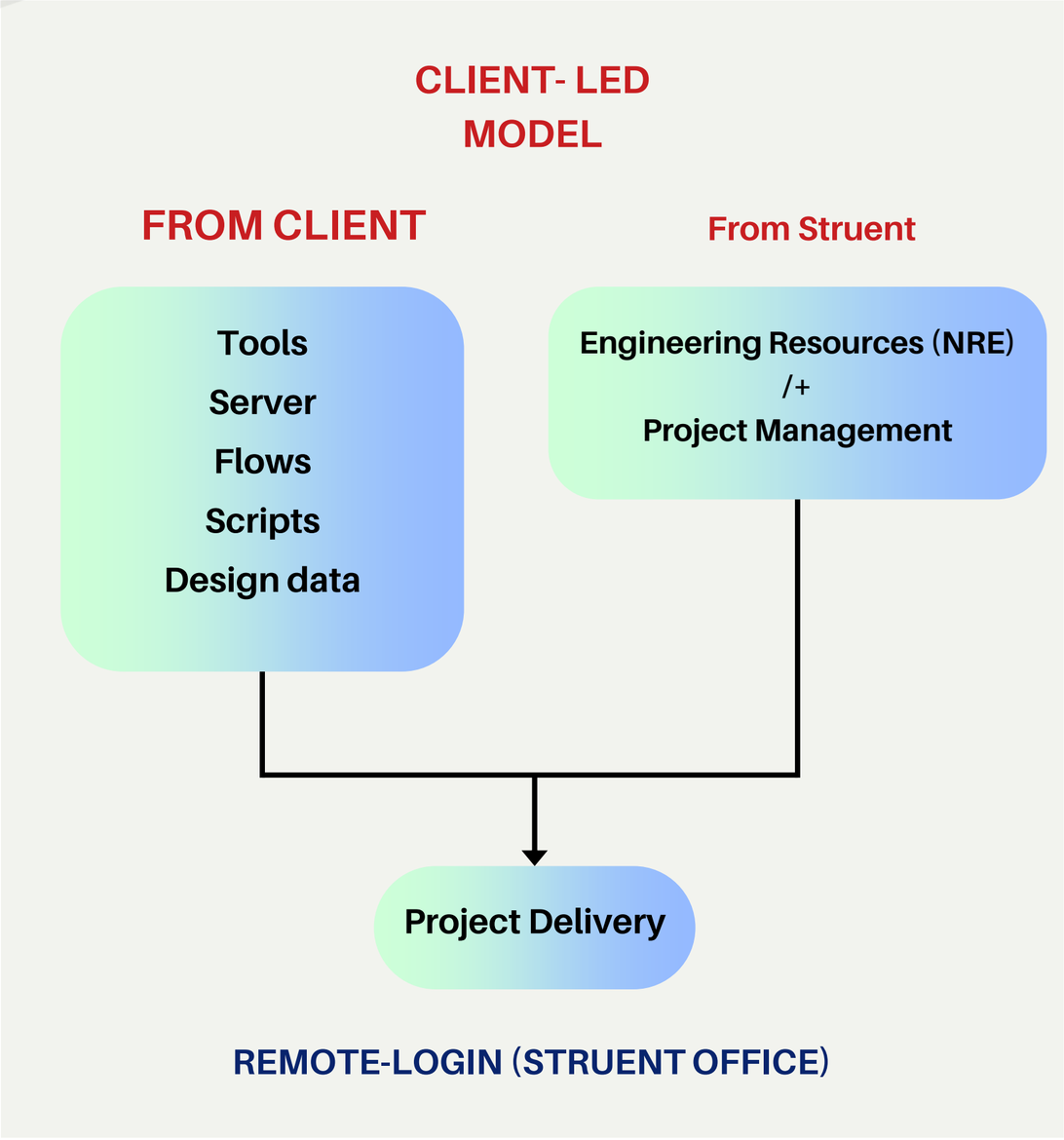
EDA TOOLS

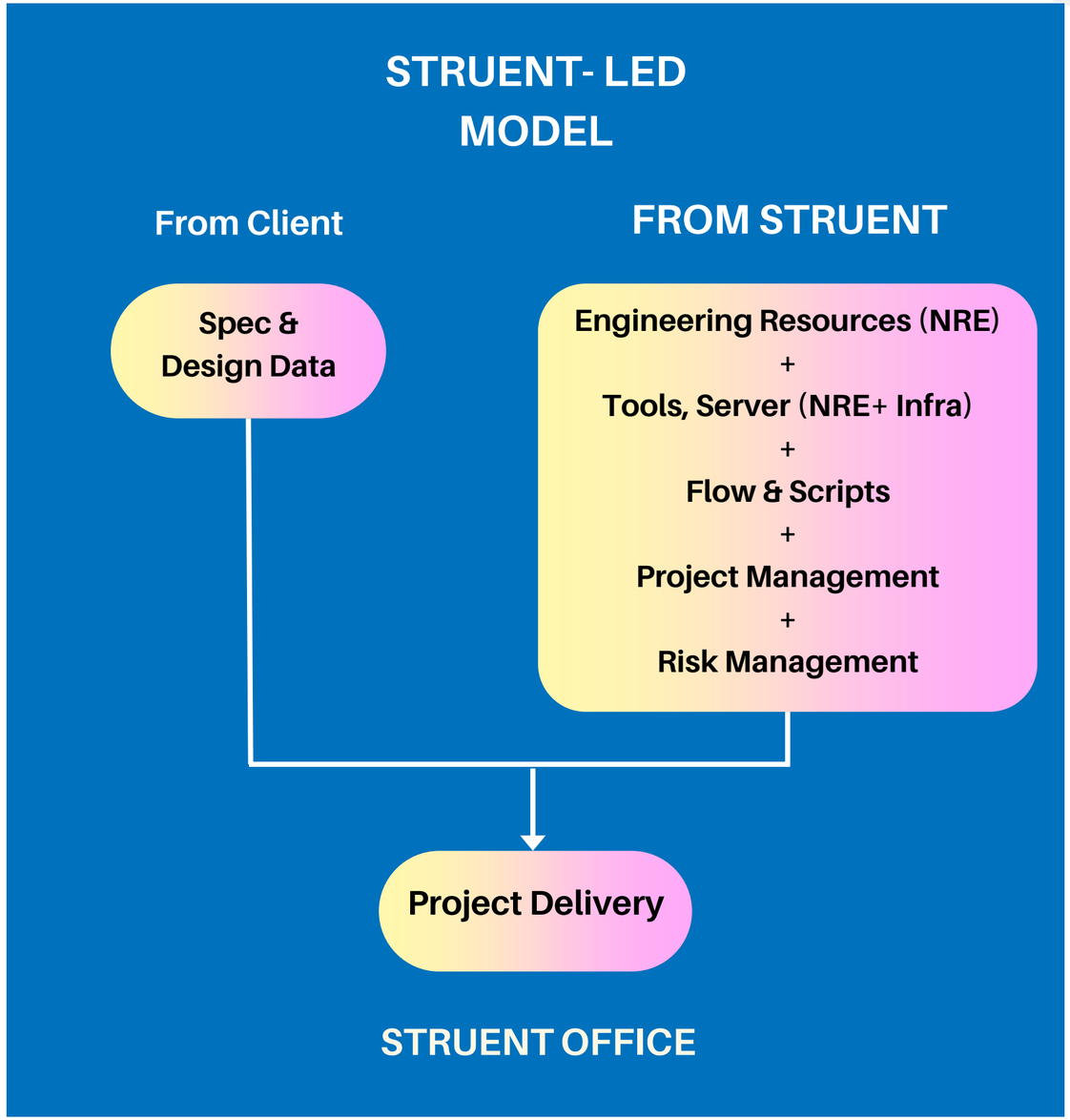
cadence

SYNOPSYS

SIEMENS

BUSINESS MODEL

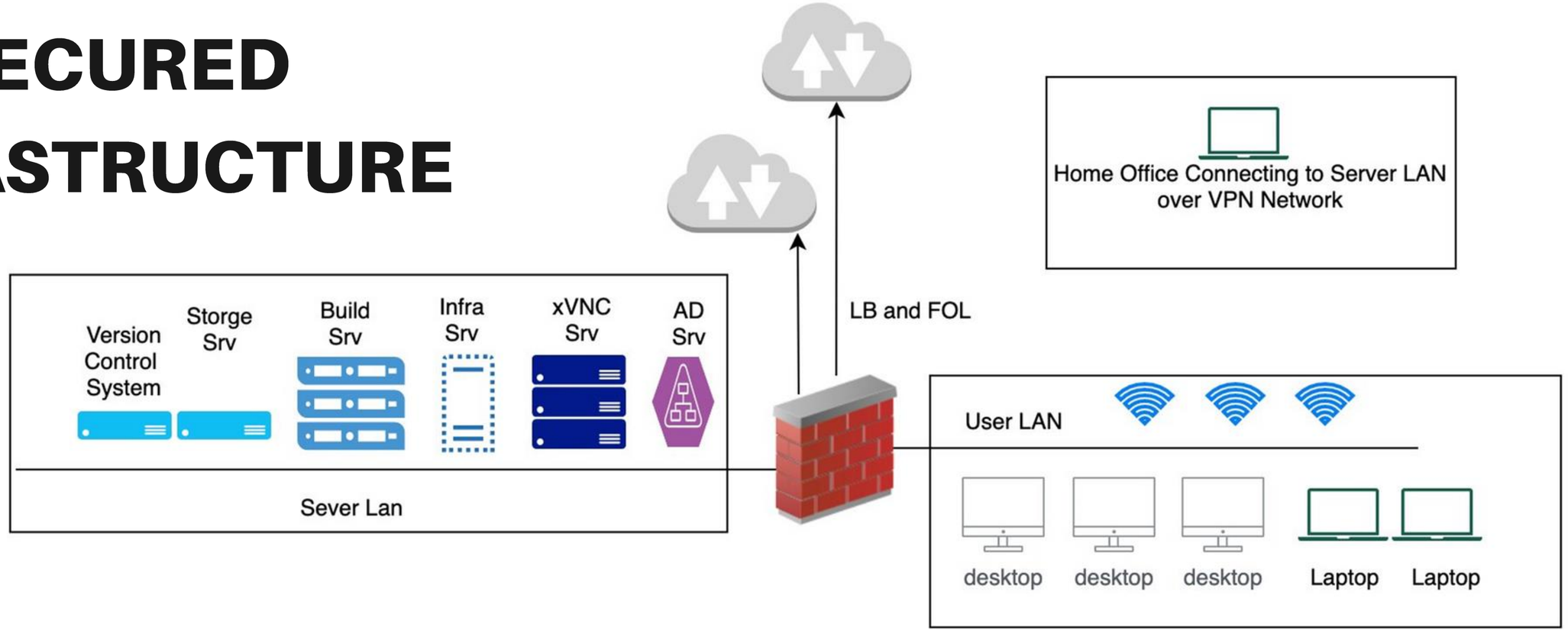




Our Billing Model – T&M, Turnkey, Milestone based

SECURED INFRASTRUCTURE

Network Diagram



Infra Server - which will be acting as NIS, DHCP, DNS server and Radius Services

Build Server - End user computing activities will be carried on these servers

Storage Server - common storage system to host Project and work area with backup

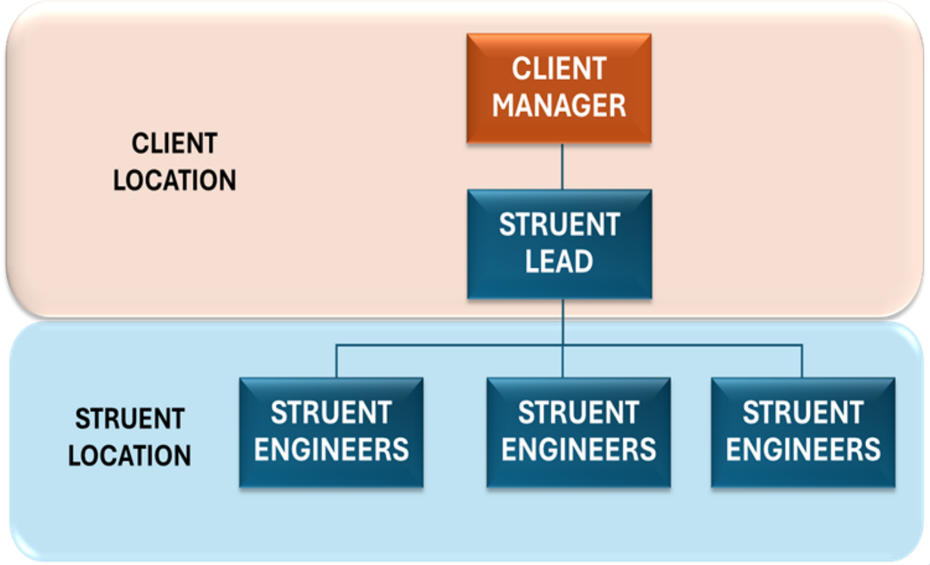
LDAP/AD Server - MS Windows Server will be used as Kerberos authentication for Single Sign On.

xVNC Servers - Each user will get their own dedicated working Virtual system, which can be used for front-end activities.

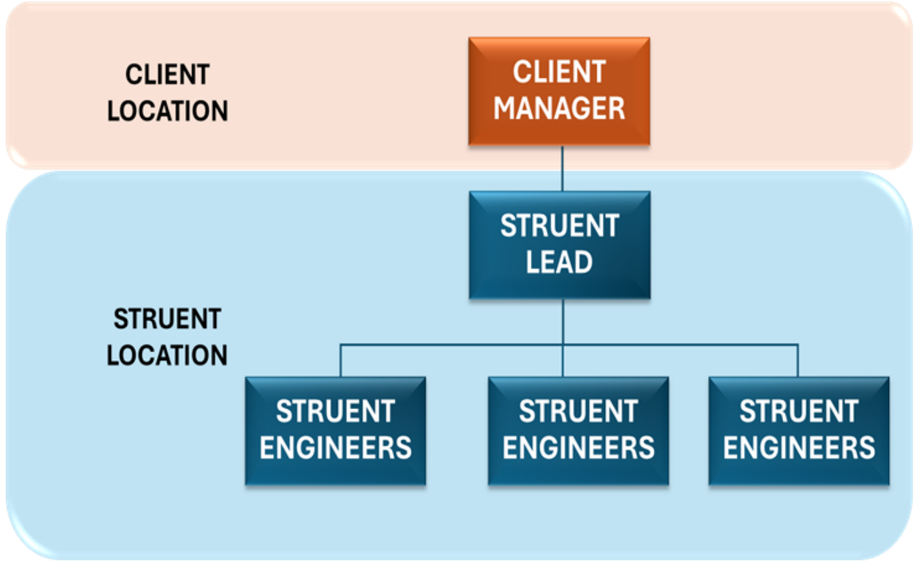
User will not be able to copy and paste or upload or download data from Server LAN

EXECUTION MODEL

LEAD-LED MODEL - HYBRID



LEAD-LED MODEL - OFFSHORE

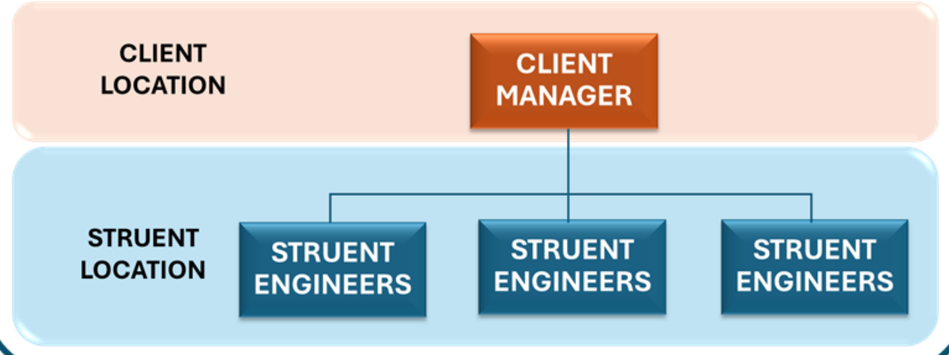


SME (20+ Yrs) Support

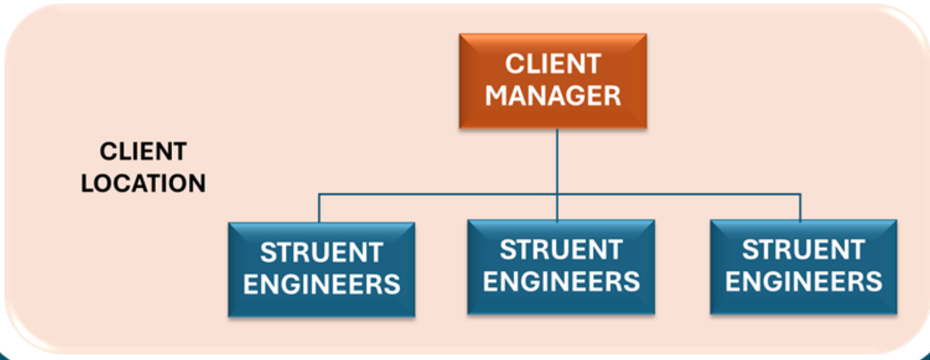
Training Support

Flow Support

OFFSHORE MODEL



ONSITE MODEL



Sample PROJECT 1

SPECIFICATIONS	
Tech node	22nm
Total Memories	395
No. of IO pins	8k+
Target Frequency	1Ghz
No. of clocks	35
No. of Blocks	1
Die Size	3 mm^2
Total instance	750k+

TOOLS USED

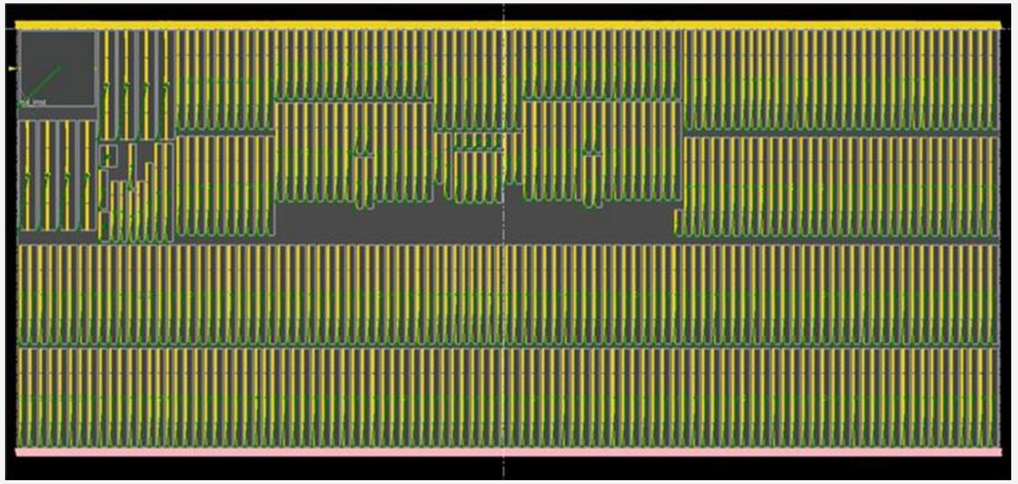
- Genus
- Oasys
- Innovus
- Aprisa

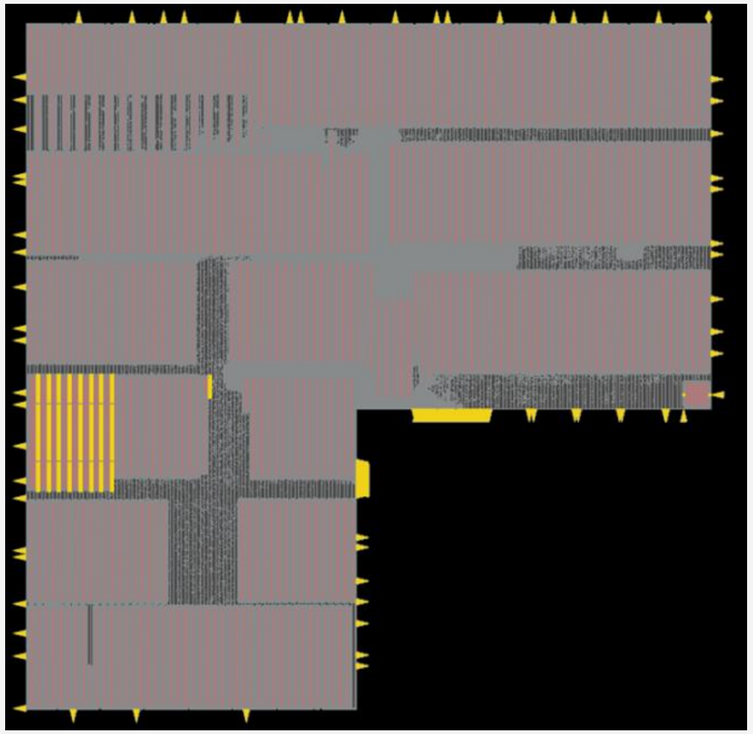
SCOPE OF WORK

- Block level implementation at 5nm and 22nm
- Synthesis with high QoR.
- Design was implemented using both Innovus and Aprisa tools
- Powerplan structure was created to accommodate memories and Via staplings was used for layer 3 and 4
- Special track requirements were implemented for 5nm.
- Handled 396 memories of different size.
- DRC and timing clean implementation

CHALLENGES

- Follow-pin structure used layer 1 & 2 causing congestion.
- Timing closure was difficult after CTS.
- Placement of boundary cells required special instruction to be followed.
- IO paths were difficult to converge due to IO latency.
- There were 8k+ IO pins needed to be handled.
- Due to the design being macro dominated the connectivity between macro and logic area had a lots of transition violations.





Sample PROJECT 2

SPECIFICATIONS	
Tech node	22nm
Total Memories	395
No. of Flops	135169
Total Chain Count	386 internal scan chains
No. of Channels	6
No. of Blocks	1
Compression Ratio	1:65
OCC	3

TOOLS USED

- Tessent
- QuestaSim

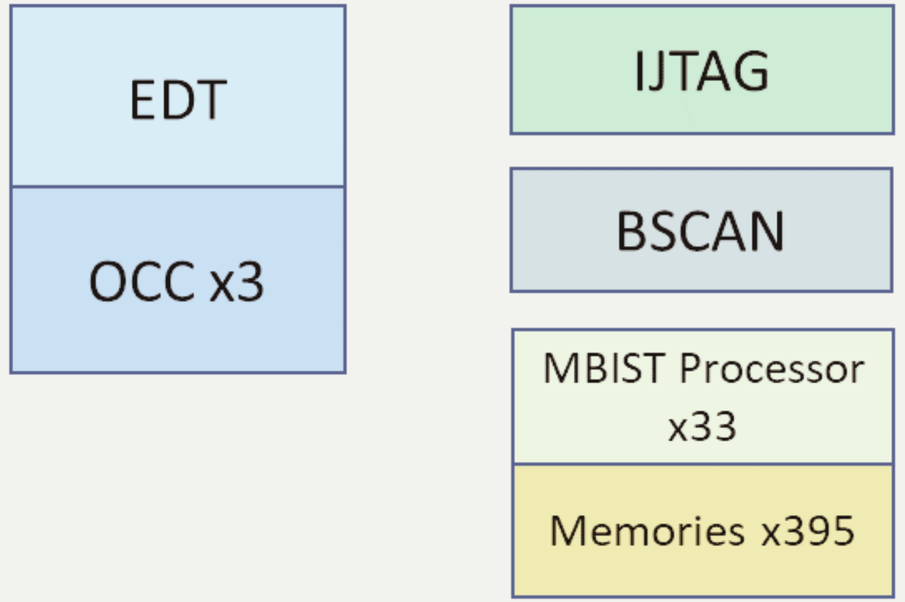
SCOPE OF WORK

- Top level MBIST insertion in RTL flow
- Top level OCC insertion and standalone
- OCC validation.
- Top level EDT insertion.
- Top level Boundary scan insertion
- Flat design final pattern generation and simulation in ZD
- Coverage analysis
- Regenerate patterns (if required) and simulate in ZD
- Timing annotated simulations

CHALLENGES

- Clock gate cell blocking the path to generated clock ref source in MBIST mode
- C6 violation – Clock interfering in capture data path resulting in miscompares in timing simulations
- Uncontrollable reset signal feeding scan cells during capture
- Unconnected logic between hookup points and primary IO in RTL
- Increased complete MBIST simulation
- Runtime.

DFT ARCHITECTURE



Spec & Architecture | Insertion | Pattern Generation

TIMELINE

Sample PROJECT 3

SPECIFICATIONS	
Tech node	7nm
Total Power Domains	9
No. of IO pads	160+
Target Frequency	1 Ghz
No. of clocks	5
No. of Macros	30
Die Size	56 mm^2
Total instance	3M+

TOOLS USED

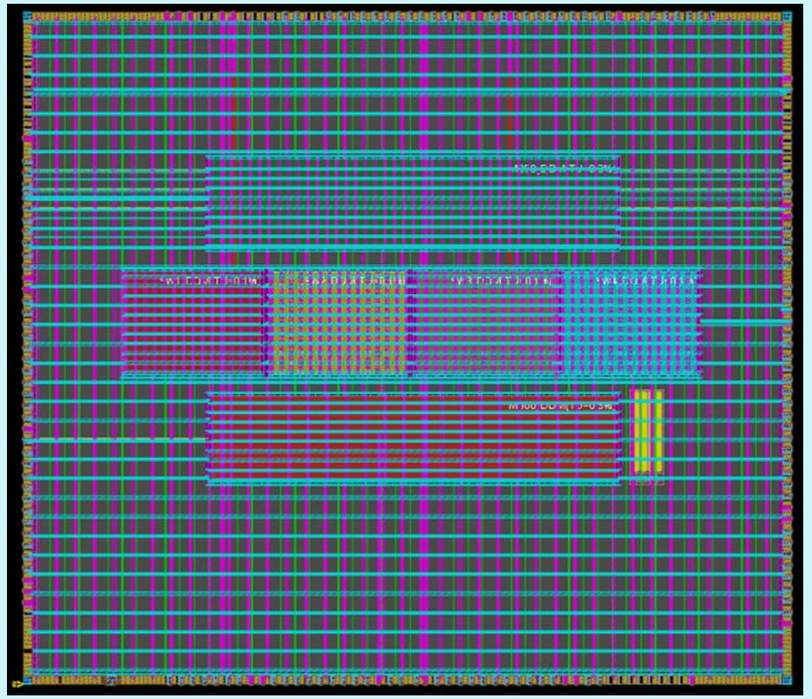
- Genus
- Innovus
- Voltus
- Tempus

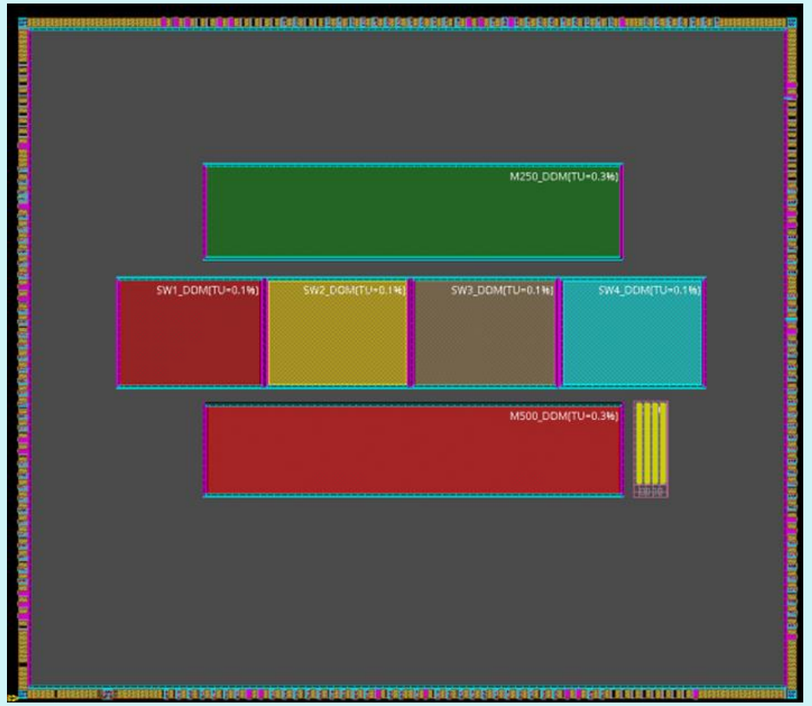
SCOPE OF WORK

- Low-power top level implementation at 7nm using UPF flow.
- Design was implemented using Innovus tool.
- Floorplan was implemented as per the requirements.
- Powerplan structure was created as per the requirements of each domain.
- Pads placement and manual routing performed.
- Switches were implemented to distribute the power.
- Low power cells were implemented as per the design (always-on and switchable domains)
- DRC and timing clean implementation.

CHALLENGES

- UPF based P&R was implemented.
- MMMC validation done for 150+ corners
- Level shifters and low power cells were placed based on power domains. Secondary PG routes were challenging.
- Site row creation for cells with different heights.
- Timing closure was difficult after CTS.
- Port issue for power switches.
- After adding power switches, rail was not aligned with the switches .





Sample PROJECT 4

SPECIFICATIONS	
Tech node	5 nm
Total Power Domains	1
No. of pins	8k+
Target Frequency	1 Ghz
No. of clocks	36
No. of Macros	2800
Die Size	150 mm^2
Total instance	4M+

TOOLS USED

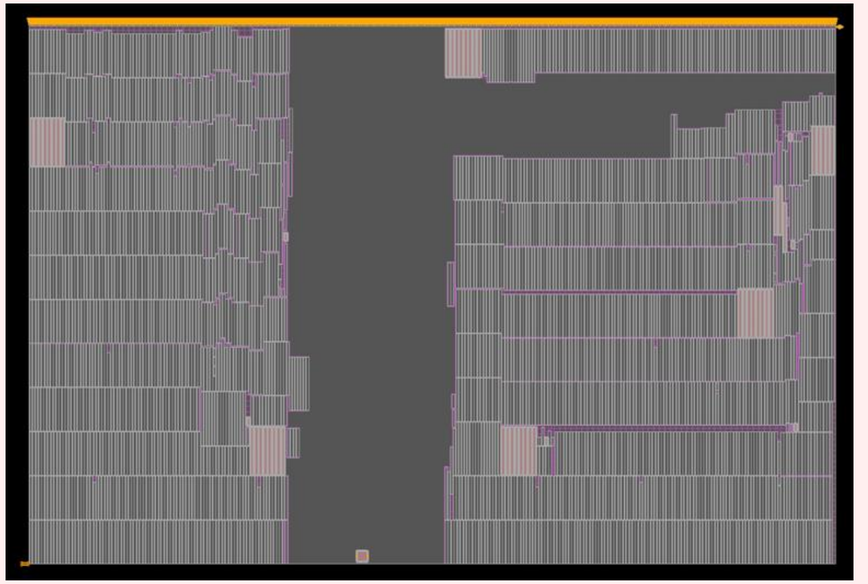
- Genus
- Innovus
- Voltus
- Tempus

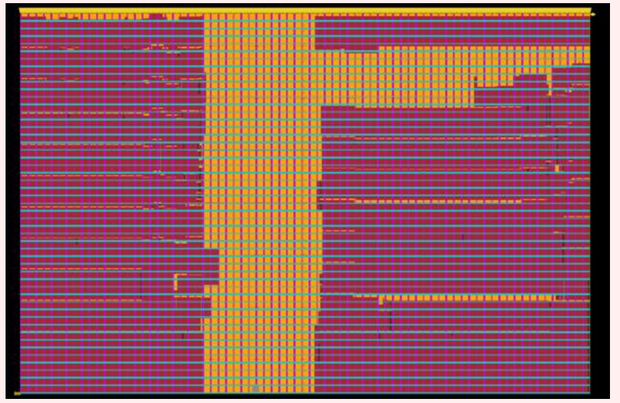
SCOPE OF WORK

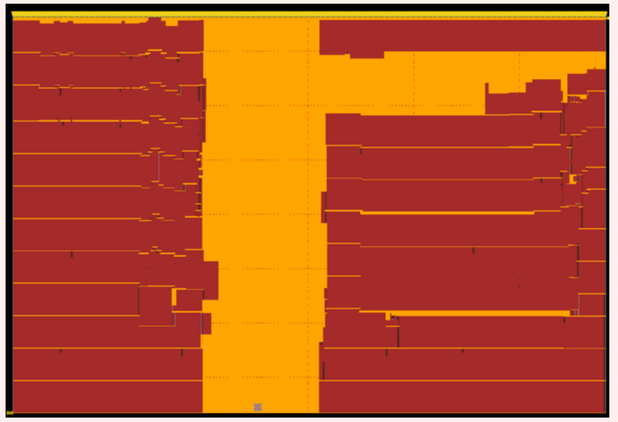
- This was a hierarchical chip where the top was partitioned to get 6 block level designs.
- Design was implemented using Innovus tool.
- Each block had 36 clocks connected from the top level with the maximum target frequency of 1Ghz.
- A robust power plan structure was created to avoid any possible IR drop due the heavy macro usage within the design.
- Timing is to be closed in AOCV analysis method.
- Powerplan should meet allowed IR drop of 2%.

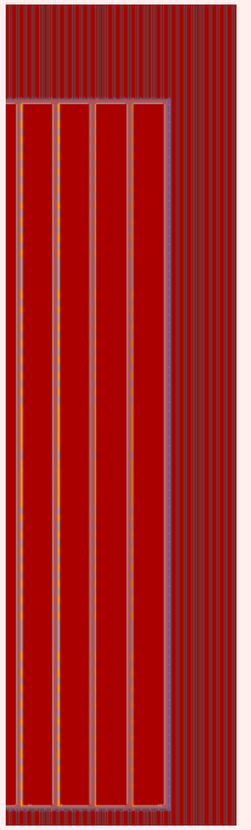
CHALLENGES

- High macro count created difficulty in finalizing floorplan.
- Had to handle 8K+ IO’s and decide on their location while maintaining reachability to all macros.
- Huge skew between blocks during CTS.
- Congestion issue around macro areas reaching the core.
- Huge datapaths had to be handled for avoiding setup violations due to datapaths.
- Long nets were causing big DRV’s in the design.









One Point Solution - Struent

- Resource Augmentation at Customer Premises
- ARM Flexible Access Member - Access to Physical Libraries
- Access to all three Major EDA tool vendors – On premise tools/Server
- Lead-led/ODC Model executed out of Struent location
- 3-way NDA with TSMC
- Packaging & Testing through 3rd party vendors
- Turn-key/Milestone based tape-out execution.
- Samsung Foundry Access (in progress)
- Library and IP procurement
- Intel Alliance Partner
- Foundry Support
- COT/Struent Flows

THANK YOU